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CROSSBAR SYSTEMS
NO. 3
TAPE RECORDER CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This circuit operates in conjunction with SD-26325-05, the trouble record trunk circuit. It controls a tape recorder used to record trouble messages, sounds an alarm when a message is coming in, and checks the parity of the incoming signal.

2. GENERAL DESCRIPTION OF OPERATION

2.01 There are three lengths of trouble messages. The short message contains 23 tone bursts; the medium, 63 bursts; and the long, 123 bursts. The trouble message is sent from the No. 3 office over a dedicated line to the trunk circuit. The trunk circuit provides line supervision and interface for the tape recorder circuit.

2.02 When a trouble message is received the trunk circuit provides a contact closure to the tape recorder circuit. This contact closure will operate the alarm and will also turn the tape recorder on if the first tone burst of the trouble message is a KP.

2.03 The tape recorder records the entire trouble message. It is turned OFF by the last tone burst of a trouble message which is an ST.

2.04 When the tape recorder circuit decodes an ST tone burst the tape recorder is turned OFF and a contact closure is provided to the trunk circuit if a message with the correct number of tone bursts has been received. This contact closure tells the trunk circuit to reverse tip and ring on the dedicated trunk that runs to the No. 3 office.

2.05 At the end of this sequence, the trunk circuit releases its contact closure which turns the alarm at the tape recorder circuit off.

SECTION II - DETAILED DESCRIPTION

1. ANALOG TO DIGITAL CONVERSION

1.01 The audio tone bursts are fed from the tip and ring inputs to the tape recorder audio input and T6 and T7 of circuit pack HU1. Circuit pack HU1 has six outputs which are normally at a logical high, +5 volts. However, if the frequency that corresponds to the outputs code is present at tip and ring that output will go to a logical low. In the remaining sections of this CD a logical low and a logical high will be referred to as a low and a high, respectively.

2. DECODING

2.01 The HU1 circuit pack outputs are decoded to the 14 possible valid combinations. This decoding produces a low

on the output of the gate associated with the pulse received and a high on all other output gates.

2.02 The decoding of the KP pulse will be presented in this paragraph. All the other decoding is essentially the same and is summed up in the table of 2.03. A KP pulse is defined as a 10 and a 2. Therefore, if the HU1 circuit pack is receiving a KP pulse, outputs 10 and 2 will be low and all the other outputs will be high. Gate AKP is an OR gate. The output is low if all the inputs are low and the output is high if any input is high. Since the 10 and 2 are connected to two of the three inputs the gate output will be low if the third input is also low. The third input is necessary to verify no other frequencies are present. This is done with gate IKP. Its output is low if all other HU1 outputs are high. The third input of AKP is the output of AKP.

2.03 Summary of decoding gates:

PULSE	CHECK PRESENCE	CHECK ABSENCE
1	A1	I1
2	A2	I2
3	A3	I3
4	A4	I4
5	A5	I5
6	A6	I6
7	A7	I7
Ø	AØ	IØ
KP	AKP	IKP
ST	AST	IST
TRL	ATRL	ITRL
MKT	AMKT	IMKT
SST	ASST	ISST
TVT	ATVT	ITVT

3. STROBE AND BLANKING

3.01 The decoding outputs are fed to NAND gates SDA and SDB which produces a high when one or more lines go low. These outputs are anded at OR gate DD. This output is connected to a chain of two one-shot nonretriggerable monostable multivibrators and the ADV gate. One shot DEL is 50 milliseconds long and one shot STROBE is 1.5-microsecond long. The chains output is added to the DD output at gate ADV. This is a 1-1/2 microsecond wide, low-going pulse which occurs 50 milliseconds after the first input to gate DD. This pulse will not occur if the DD input does not last for at least 50 milliseconds. Short operations of HU1 outputs will therefore not trigger the circuitry that follows. The ADV gate output called ADV-0, is fed to another one-shot called BLK. This one-shot produces a blanking function which does not allow any outputs closer than 70 milliseconds apart. The output gate ADV is labeled ADV-0, or the advance pulse.

3.02 The strobe output is also taken to one-input of NAND gate RES. It provides the same strobing function as it did at the ADV gate. The other input of the RES gate is high when one or both inputs of gate TKP are low. This occurs when a KP or a TRL is decoded. The output of gate RES is labeled R-0 or reset.

3.03 The output of gate STD is high when AST-0 is low. This occurs when an ST burst is received. At gate ST-0 the start detection is anded with the strobe using the same techniques discussed previously to produce ST-0 or start-low.

4. PARITY COUNTING

4.01 The reset low (R-0) pulse is inverted at hex inverter RES and fed to the units and tens counters. When this line goes high it will reset the counters to zero. When the reset line goes low, the counters are ready to begin counting.

4.02 Each time the ADV-0 line goes low the units counter will count one count. The units counter has four BCD outputs.

4.03 When the units counter counts to ten a pulse is delivered to the input of the tens counter. The tens counter also has a four terminal BCD output.

4.04 When the tens counter counts ten times (to 100) a pulse is delivered to the HUND flip-flop via the hex inverter HUNI. The 1 output of this flip-flop is low from reset to 99 count and high from 100 count to reset. The 0 output of this flip-flop is the inverse of the 1 output.

4.05 Every time the units counter is at a two count (2, 12, 22, 32, etc) the output of the strobed NOR gate two is high. The two count is decoded by this two gate

and hex inverter unit. Note that terminal three of the two gate, which is the strobe input, is held high at all times.

4.06 Hex inverters TEND, TENC, and TENA provide appropriate inversion for decoding.

4.07 During the count of 22 all inputs of the eight input NAND gate SPA go high thereby making the output, designated SPA-0, go low.

4.08 During the count of 62 all inputs of MPA go high thereby making the output, designated MPA-0, go low.

4.09 During the count of 122 all inputs of LPA go high thereby making the output, designated LPA-0 go low.

5. CONTROL AND OUTPUT CIRCUITRY

5.01 Before a tone burst trouble record is sent from the trunk circuit a make-contact is closed by the trunk circuit across lines RV3 and RV4 which runs to the tape recorder circuit. This connects the +5 volts on RV3 to RV4. The RV4 supplies power to the coil of relay B and to the trouble record alarm A1.

5.02 The first tone burst to arrive should always be a KP or a TRL pulse and will cause line R-0 to go low for 1.5 microseconds. This will cause the output of the "control" flip-flop to go low. When this occurs the output of buffer-driver RFCD will be driven high. Since this output is connected to the coil of relay A, it will cause the contact of relay A to make.

5.03 At this point the contacts of relays A and B are both made. Since these contacts are wired in series and to the tape recorder start-stop control the tape recorder will begin recording what is arriving over tip and ring.

5.04 At the end of a valid trouble message an ST pulse is sent causing line ST-0 to go low for 1.5 microsecond when the AST-0 goes high. This will cause one-shot multivibrator TIMER to go high for about 100 milliseconds. If a valid number of tone bursts have been counted (ie, LPA-0, MPA-0, or SPA-0 are low) the output of gate PAR will be high enabling the TIMER pulse to pass through and be inverted by the REV gate. The output of this gate is inverted by buffer-driver REV-I and is connected to relay coil C. The make-contacts of relay C are thus closed for about 100 milliseconds. This contact closure is across RV1 and RV2. These lines run to the trunk circuit and tell it to reverse tip and ring to the No. 3 office.

5.05 As soon as ST-0 goes low the "control" flip-flop is reset and relay A is released, turning off the tape recorder as soon as AST-0 goes high.

5.06 At this time the contact closure across RV3 and RV4 is released by the trunk circuit turning off the alarm A1 and releasing relay B.

5.07 The switch in the alarm A1 line will disconnect the alarm should it become undesirable.

5.08 An additional ALM gate operates the A1 relay which follows the A relay.

6. POWER CIRCUITRY

6.01 The 110 volts ac is supplied to the tape recorder ac input and to the +5 volt power supply. The lines are fused per conventional practice with F1 and F2. A lamp PS is provided as a pilot light.

6.02 Minus 48 volts is supplied to circuit pack HU1 from frame battery.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The tip and ring input levels must be no greater than -3 dBm and no less than -16 dBm.

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Packages

Designation	Meaning
HU1	Two-out-of-six outpulser frequencies analog to digital converter.

3. FUNCTIONS

3.01 Records trouble records on a tape cassette in audio tone burst format.

3.02 Checks for valid trouble records and verifies same via a contact closure to the trunk circuit.

3.03 Sounds an audible alarm during the time a trouble record is being received.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon should be followed:

(a) Trouble Record and Trunk Circuit - SD-26327-05.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Adjust PS-1 to produce +4.9 volts to +5.1 volts out.

5.02 Connect the Trunk Circuit - SD-26327-05 to the tape recorder circuit. The tape recorder should be loaded with a tape cassette. Use a -2 dBm ± 1 dBm input level.

5.03 Activate the trunk circuit to produce a valid short, medium, and long pulse. The tape recorder circuit must return tip and ring properly to the trunk circuit.

5.04 Simulate several trouble records with an incorrect number of tone bursts. The tape recorder circuit must not return tip and ring.

5.05 Repeat steps 5.03 and 5.04 with an input level of -16 dBm ± 1 dBm. The results must be the same.

5.06 During steps 5.02 through 5.05 the Sonalert must sound during recording and the tape recorder must begin recording when KP is received and stop when ST is received. The input level control of the recorder must be set as appropriate.

5.07 The alarm switch, when placed in the "off" position must disable the Sonalert.

5.08 The pilot lamp must light when power is applied to the unit.

5.09 Instead of using a line circuit a tape recorder with the appropriate recordings may be used for these tests. The input-output lines must be also monitored if the recorder is used.

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