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CROSSBAR SYSTEMS
NO. 3
LOOP AND LEAK
TEST CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The loop and leak test circuit is designed to simulate various marginal calling customers line conditions by imposing those conditions on the tip and ring using a cord patching arrangement. This circuit is used in conjunction with the test frame originating or incoming test lines in a dial pulse mode. Several critical operational tests are performed on the L relay of the originating register, and incoming register.

1.02 A precision pulsing source such as the 3A pulse generator or equivalent is required to provide dial pulses at different speeds for the various critical conditions.

1.03 Simulation of surge tests are not provided in this circuit. Refer to Manufacturing Test Requirements note in the originating register or incoming register schematic.

2. GENERAL DESCRIPTION OF OPERATION

ORIGINATING TEST LINE - (OTL)

2.01 A test call using the OTL is started by the test frame by closing a loop across the tip and ring leads to the line location. This operates a line relay which then puts in requests for the marker to select an originating register. When the originating register is seized and linkage is set up between line location and the originating register, dial tone is heard indicating dialing can start.

2.02 The entire loop at this time is under control of a back contact of the dialer in the pulsing source to the L relay in the originating register. This is done through the cord patching arrangement that includes this circuit as part of the overall loop.

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2.03 The patching cords are used as follows:

(a) From the pulsing source OUT jack to jack DIAL in this circuit.

(b) From the OUT jack of this circuit to a convenient SP jack on frame upright.

(c) At the test frame; from jack SP to jack ORDL.

2.04 The LL switch is set to one of eight positions depending on type of test to be performed.

2.05 After dial tone is heard the ST key is operated to impose the desired loop condition across the tip and ring.

2.06 The pulse generator is now started to pulse at desired speed, percent break, and digits.

2.07 As pulses are generated the loop and leak conditions are imposed on tip and ring leads to L relay of A register.

2.08 Loop conditions are imposed when pulsing contact of pulsing source is closed.

2.09 Leak conditions are imposed when pulsing contact of pulsing source is open.

2.10 When all digits are pulsed and call is processed, the ST key can be returned to normal.

INCOMING TEST LINE - (ITL)

2.11 The test frame using its ITL is started by closing a loop across the tip and ring leads to the A relay of an incoming trunk. The operated A relay starts to the incoming register link circuit which in turn seizes an incoming register.

2.12 Operation continues from this point as described in 2.02 to 2.10 except dial tone is not heard as start dial signal from incoming register and jack IRDL is used in place of jack ORDL.

SECTION II - DETAILED DESCRIPTION

1. PRELIMINARY OPERATION

1.01 Patch cords must be utilized to put this circuit into a working loop controlled by the test frame before test call is started:

From	To
Pulse Generator OUT Jack	DIAL Jack
Miscellaneous Circuit SP Jack	OUT Jack

1.02 At the test frame a cord is patched from its ORDL or IRDL jack to jack SP in miscellaneous circuit.

1.03 The test frame must be prepared to test one of the following equipments:

(a) Originating Registers, (Noncoin)

(b) Originating Registers, (Coin)

(c) Incoming Registers.

1.04 The LL switch is set to desired position and keys TD and CN operated accordingly.

1.05 The ST key is not operated until dial tone is heard.

1.06 The 3A pulse generator or equivalent is prepared for proper pulsing.

2. OPERATION

2.01 With LL switch in position 1, 2, 4, 6, 7, or 8 and ST key is not operated, resistor LD with a value of 3480 ohms is the loop resistance when seizing a register.

2.02 With LL switch in position OFF, 3, or 5 and ST key not operated there is zero resistance in the loop when seizing a register.

2.03 The loop condition presented between pulsing source and register is apparent from the ring of jack DIAL to ring of jack OUT for one side and tip of jack DIAL through LL switch position to tip of OUT jack for other side.

2.04 The leak condition presented to L relay being tested is from tip of jack OUT through LL switch position to ring of jack OUT.

Note: The leak condition consists of resistance and a bridge consisting of capacitors and inductors.

2.05 After test frame is started and the register is seized, key ST is operated followed by operation of key ST in pulse generator. As the pulse generator is pulsing (opening and closing), the marginal condition as set on LL switch is imposed across the line.

3. MARGINAL LINE CONDITIONS

3.01 There are 15 different marginal combinations available under six line conditions depending on LL switch setting and pulsing speed and percent break.

3.02 Using Table A for the various combination, the following line conditions are applied:

CONDITION A

3.03 This tests the ability of the register RA relay to hold over dial pulses. It also tests the bias winding strength and adjustment of the L relay.

CONDITION B

3.04 This tests the ability of the SR relay in the originating register and the abandon call timer in the incoming register to hold over dial pulses. It also tests the bias winding of the L relay

CONDITION C

3.05 This tests that the registers L relay back contact closure is long enough to register a digit in the counting circuit.

CONDITION D

3.06 This tests the register L relay circuit for proper wiring.

Note: Key TD must be operated.

CONDITION E

3.07 This tests that the L relay releases fast enough to operate RA relay so that the first digit is recorded in counting circuit.

CONDITION F

3.08 This tests that the register L relay provides sufficient front contact closure to insure proper registration of digit registers in the minimum time between digits.

TABLE A

LINE CONDITIONS

Tests	Condition	LL Position	PPS/% Brk	Loop Ohms	Leak Ohms	Bridge
Originating Register Noncoin	A	1	7-50	2140	5020	None
	B	1	7-80	2140	5020	None
	C	3	15-65	0	10,000	Two: 2.16 MF ISW 274F Indr ISW 1620 Ohms
	D	4	15-65	300	---	Two: 2.7 MF ISW 274F Indr ISW 1620 Ohms and 3.24 MF
	E	5	24-55	0	30,000	3.24 MF ISW 600 Ohms
	F	6	24-70	1650	---	None
Originating Register Coin (Operated CN Key)	A	2	7-50	3010	10,070	None
	B	2	7-80	3010	10,070	None
	C	3	15-65	0	10,000	2.16 MF ISW 274F Indr ISW 1620 Ohms
	F	6	24-70	2300	---	None
Incoming Register	A	7	7-50	4530	16,030	None
	B	7	7-80	4530	16,030	None
	C	5	24-55	0	30,100	3.24 MF ISW 600 Ohms
	F1	8	24-70	4270	---	None
	F2	OFF	24-70	0	---	None

4. TYPICAL LINE CONDITION

4.01 Assume we are testing the L relay of an originating register with a noncoin call. (Table A, Condition A.) The LL switch is set to position 1. The pulse generator is set to pulse at 7 pulses per second with 50 percent break.

4.02 After test frame is started, ST key is operated and the pulse generator is started, the following condition is imposed on the line.

LOOP

4.03 When pulsing contact is closed a loop is presented from tip of jack DIAL to tip of jack OUT and on the L relay of the register for half of the loop. The other half of the loop is from the closed contact of pulsing contact to ring of DIAL jack to position 1 on section 2 of LL switch through resistor LO (2150 ohms) to position 1 on section 1 of LL switch to ring of OUT jack and on to L relay of the register.

LEAK

4.04 When pulsing contact is open a leak condition is presented to the L relay of the register from tip of jack OUT through resistor L1 (2870 ohms) through resistor LO (2150 ohms) to position 1 on section 1 of LL switch to ring of jack OUT. The total leak resistance is 5020 ohms.

4.05 There is no bridge involved with this condition.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

2.01 Switch

Designation	Meaning
LL	Loop and Leak

2.02 Keys

Designation	Meaning
CN	Coin
ST	Start Test
TD	Test Condition D

3. FUNCTIONS

3.01 Provides jacks for access so as to be patched into a loop from the test frame to a pulse generator.

3.02 Provides a rotary switch to select various line conditions to be simulated and imposing them toward L relay of originating registers or incoming registers.

3.03 Provides an array of resistors, capacitors, and inductors in different positions of LL switch.

3.04 Provides loop and leak conditions for originating registers under following pulsing conditions:

Pulses Per Second	Percent Break	
7	Minimum	(Noncoin)
7	Maximum	(Noncoin)
15	Minimum	(Noncoin)
15	Maximum	(Noncoin)
24	Minimum	(Noncoin)
24	Maximum	(Noncoin)
7	Minimum	(Coin)
7	Maximum	(Coin)
15	Minimum	(Coin)
15	Maximum	(Coin)

3.05 Provide loop and leak conditions for incoming registers under following pulsing conditions:

Pulses Per Second	Percent Break
7	Minimum
7	Maximum
24	Minimum
24	Maximum

4. CONNECTING CIRCUITS

4.01 This circuit has no external wiring.

4.02 By using cords, this circuit can be patched into a pulsing source and test frame.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The loop and leak test circuit shall be capable of performing all functions covered in this Circuit Description and meeting all manufacturing test requirements in the schematic drawing.

5.02 The loop and leak test circuit is not capable of applying surge tests. When reference to surge testing ability is required refer to originating register schematic, SD-26385-01 or incoming register schematic, SD-26386-01.

5.03 All operations shall be made with voltages within -45 volts minimum to -50 volts maximum.

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