CPS A152
MF CHANNEL DETECTOR

APPARATUS LIST

CAPACITOR

DESIG	CODE
C1.0	~~5428~~ 702G,0.5Ω
C1.1	~~5428~~ 702G,0.5Ω

DIODE

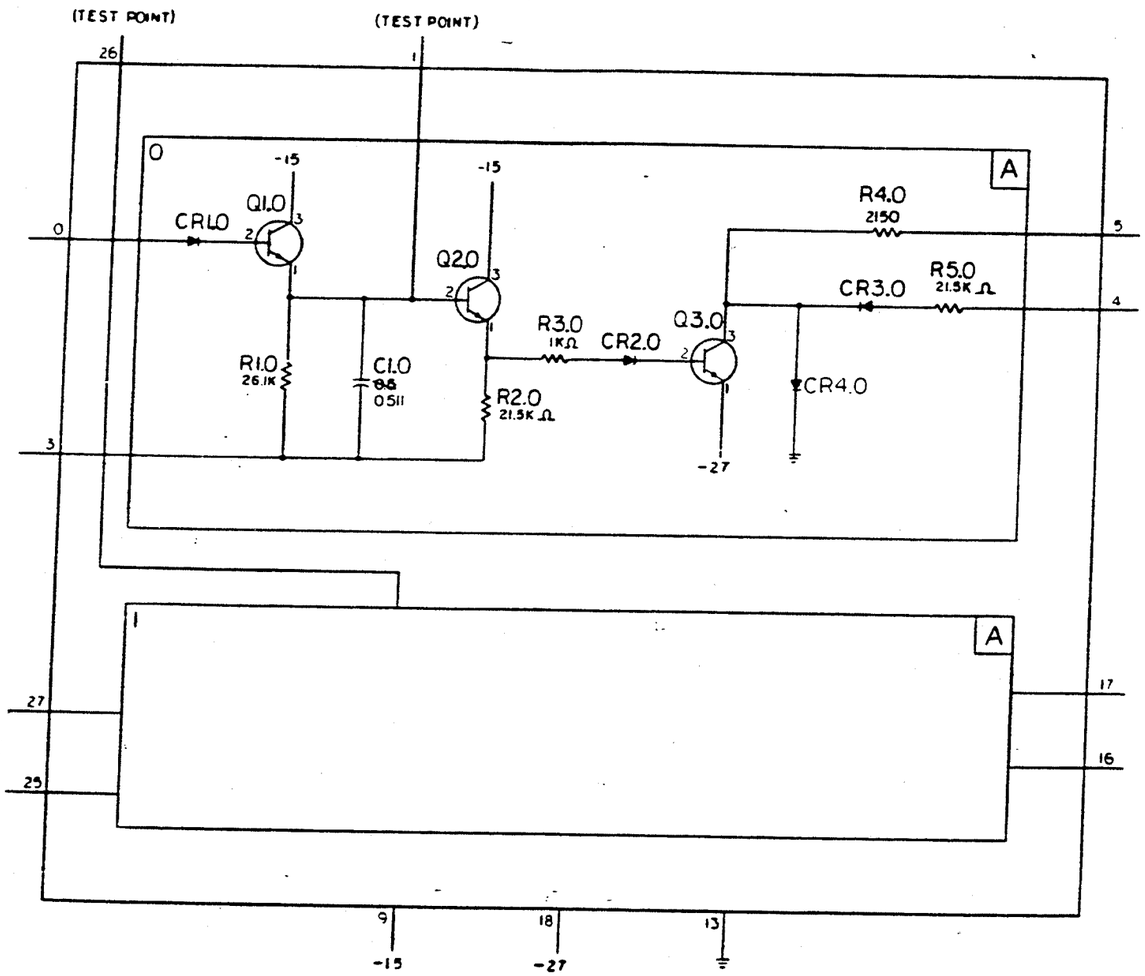
DESIG	CODE
CR1.0	~~3464~~ 533G
CR1.1	~~3464~~ 533G
CR2.0	~~3464~~ 533G
CR2.1	~~3464~~ 533G
CR3.0	~~3464~~ 458C
CR3.1	~~3464~~ 458C
CR4.0	(ZZ) 458C (ZY) 4478
CR4.1	(ZZ) 458C (ZY) 4478

RESISTOR

DESIG	CODE
R1.0	~~2974~~ KS-20616 L1A,26.1KΩ
R1.1	,26.1KΩ
R2.0	,21.5KΩ
R2.1	,21.5KΩ
R3.0	,1KΩ
R3.1	~~2974~~ KS-20616 L1A,1KΩ
R4.0	~~TYPE 2360~~ KS-20810 L1A,215Ω
R4.1	~~TYPE 2150~~ KS-20810 L1A,215Ω
R5.0	~~2974~~ KS-20616 L1A,21.5KΩ
R5.1	~~2974~~ KS-20616 L1A,21.5KΩ

TRANSISTOR

DESIG	CODE
Q1.0	29A
Q1.1	
Q2.0	
Q2.1	
Q3.0	
Q3.1	29A



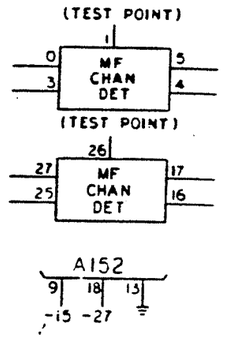
NOTES:

1. HORIZONTAL MOUNTING CENTER 0.8 INCH.
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS,
   CAPACITANCE VALUES ARE IN MICROFARADS,
   VALUES PRECEDED BY THE SYMBOL + (PLUS)
   OR - (MINUS) ARE IN VOLTS.

SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT PACK CODE REQUIREMENTS PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		A152 A-858282 905A OR 905B
SERIES NO. IDENT.	FOR LATEST CLASS "A" CHANGE	3
	FOR CURRENT MANUFACTURE	5

SYMBOL



DESCRIPTION

THIS CIRCUIT PACK CONTAINS TWO CHANNEL DETECTORS. THREE PWB'S ARE NEEDED FOR THE SIX CHANNELS IN AN MF RECEIVER.

PURPOSE:
A CHANNEL DETECTOR RESPONDS TO AN AC SIGNAL SELECTED BY A SERIES TUNED CIRCUIT IN THE MF SIGNAL FILTER. IT CONVERTS THIS AC SIGNAL TO A DC SIGNAL SUITABLE FOR OPERATING A SCANNER D FERROD.

INPUT AND OUTPUT:
THE INPUT AC SIGNAL SELECTED AT THE TAP OF ONE OF THE SERIES RESONANT CIRCUITS IN THE MF SIGNAL FILTER SHOULD BE ABOUT 10 VOLTS RMS. THE 0 CIRCUIT ON EACH PWB USES TERMINALS 0 AND 3 FOR INPUT AND THE 1 CIRCUIT USES 27 AND 25. TERMINALS 3 AND 25 ALSO RECEIVE THE DC BIAS FROM THE GUARD DRIVER ON CPS A149. THE BIAS LEVEL IS APPROXIMATELY -31 VOLTS WHEN NO SIGNAL OR MF PULSING FREQUENCIES ONLY ARE PRESENT. IF OTHER FREQUENCIES ARE PRESENT, IT WILL DROP TO APPROXIMATELY -41 VOLTS. TERMINALS 5 AND 17 CONNECT THROUGH FERRODS TO GROUND TO PROVIDE OUTPUT SIGNALS FOR THE 0 AND 1 CIRCUIT RESPECTIVELY. WHEN AN MF TONE IS PRESENT AND NON-MF TONES ARE ABSENT, THE FERROD IS SATURATED AND ITS OUTPUT IS 0. FOR NO TONE OR TONE IN THE PRESENCE OF NOISE, NEGLIGIBLE CURRENT FLOWS, THE FERROD IS NOT SATURATED, AND ITS OUTPUT IS 1. THE OUTPUTS ON TERMINALS 4 AND 16 ARE TIED TOGETHER FOR ALL MF CHANNEL DETECTORS, AND WHEN TWO OR MORE CHANNEL DETECTORS ARE OPERATED, AN INPUT SIGNAL OF ABOUT -18 VOLTS IS TRANSMITTED TO TERMINAL 27 OF THE MF SP TIMER, CPS A153.

OPERATION:
Q1 RECTIFIES THE INPUT AC SIGNAL WHICH IS FILTERED TO DC BY R1 AND C1. Q2 DECOUPLES THE FILTER FROM Q3. WHEN THE FILTER VOLTAGES (AS SEEN AT THE EMITTER OF Q2) PLUS THE BIAS VOLTAGE FROM THE GUARD DRIVER CPS A149 BECOMES MORE POSITIVE THAN THE -27 VOLTS AT THE EMITTER OF Q3, Q3 WILL CONDUCT TO DRAW CURRENT FROM GROUND VIA THE ASSOCIATED FERROD AND CPS A153. CR1 AND CR2 LIMIT EXCESSIVE REVERSE VOLTAGES ACROSS THE BASE-EMITTER JUNCTIONS OF Q1 AND Q3. CR3 DECOUPLES THE OUTPUT TO CPS A153 FROM SCANNER OUTPUT. R4 LIMITS FERROD CURRENT AND R5 FORMS ONE BRANCH OF A PARALLEL ADDING NETWORK. CR4 IS USED TO CLIP MOMENTARY TRANSIENTS.

CPS A152

ISSUE 95D

CIRCUIT PACK SCHEMATICS (2) SD-1A102-01-B152

AT&T BELL LABORATORIES 6S

SD-1A102-01-B152

DRAWING ISSUE

1	
2A	
17D	
22D	
24A	
55D	
56D	

CPSA246
CHARACTER ASSEMBLER/IDENTIFIER (HOF)

APPARATUS LIST

CAPACITOR

DESIG	CODE
C1	535 JR,.25
C2	535 JR,.25
C3	535 JP,.05
C4	(YS) D10C60MU DICKSON CO.,10
C4	(YY) 606C,10
C5	(YS) D10C60MU DICKSON CO.,10
C5	(YY) 606C,10
C6	(YS) D1R0B60MU DICKSON CO.,1.0
C6	(YY) 605B,1.0

SHIFT REGISTER

DESIG	CODE
SR1	1A

TRANSISTOR

DESIG	CODE
Q1.0	29A
Q1.1	29A
Q1.2	29A
Q2	29A
Q3.0	27A
Q3.1	27A
Q3.2	27A

DIODE

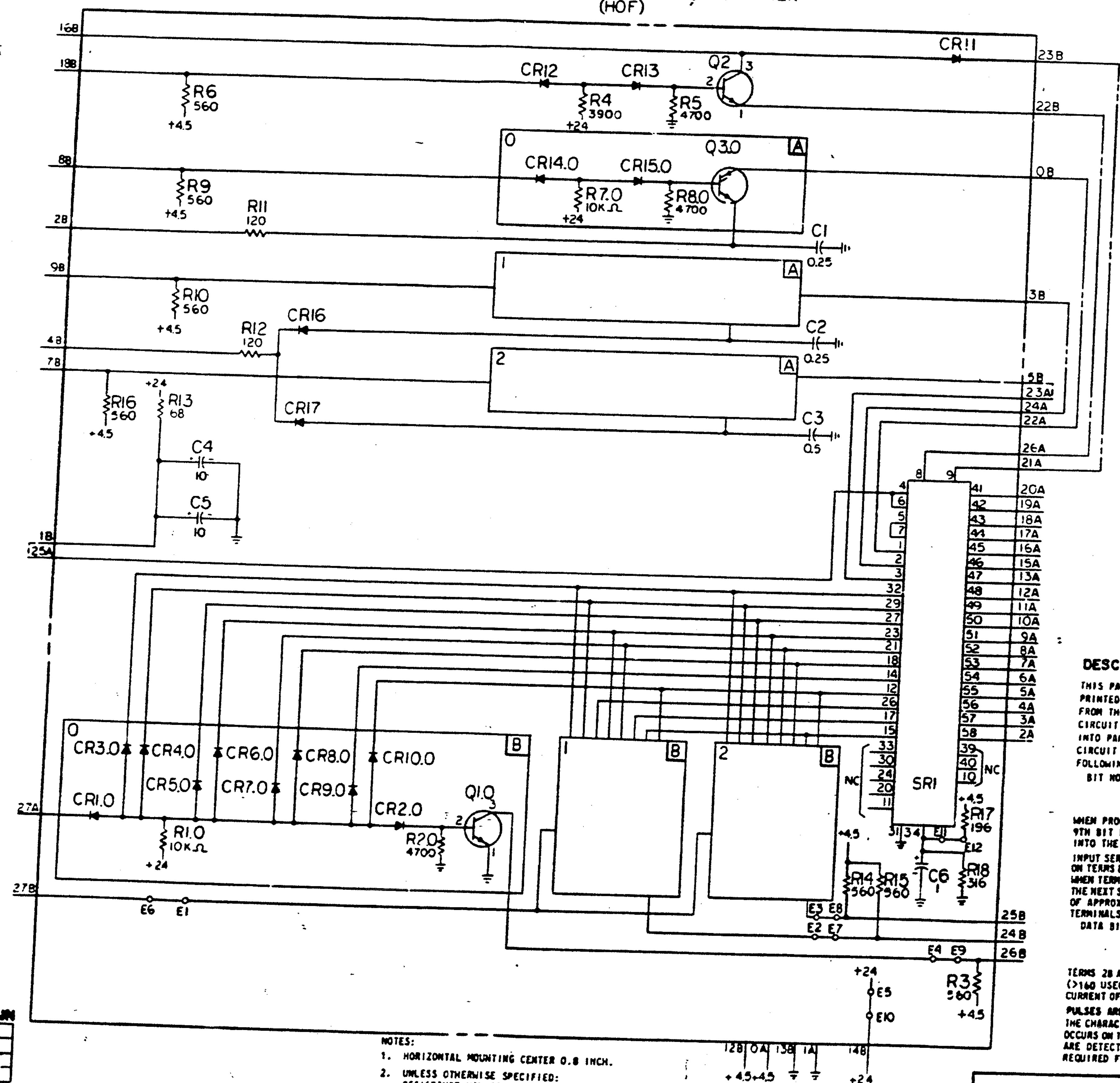
DESIG	CODE
CR1.0	(YQ) 458C, (YR) 447A
CR1.1	(YQ) 458C, (YR) 447A
CR1.2	(YQ) 458C, (YR) 447A
CR2.0	449A
CR2.1	449A
CR2.2	449A
CR3.0	(YQ) 458C, (YR) 447A
CR3.1	
CR3.2	
CR4.0	
CR4.1	
CR4.2	
CR5.0	
CR5.1	
CR5.2	
CR6.0	
CR6.1	
CR6.2	
CR7.0	
CR7.1	
CR7.2	
CR9.0	
CR9.1	
CR9.2	
CR9.0	
CR9.1	
CR9.2	
CR10.0	
CR10.1	
CR10.2	(YQ) 458C, (YR) 447A
CR11	446A
CR12	(YQ) 458C, (YR) 447A
CR13	449A
CR14.0	(YQ) 458C, (YR) 447A
CR14.1	(YQ) 458C, (YR) 447A
CR14.2	(YQ) 458C, (YR) 447A
CR15.0	449A
CR15.1	449A
CR15.2	449A
CR16	446A
CR17	446A

RESISTOR

DESIG	CODE
R1.0	KS-16645 L2, 10KΩ
R1.1	10KΩ
R1.2	10KΩ
R2.0	4700
R2.1	4700
R2.2	4700
R3	560
R4	3900
R5	4700
R6	560
R7.0	10KΩ
R7.1	10KΩ
R7.2	10KΩ
R8.0	4700
R8.1	4700
R8.2	4700
R9	560
R10	560
R11	120
R12	120
R13	68
R14	560
R15	560
R16	KS-16645 L2, 560
R17	257A KS-20616 L1A,196
R18	257A KS-20616 L1A,326

CURRENT DRAIN

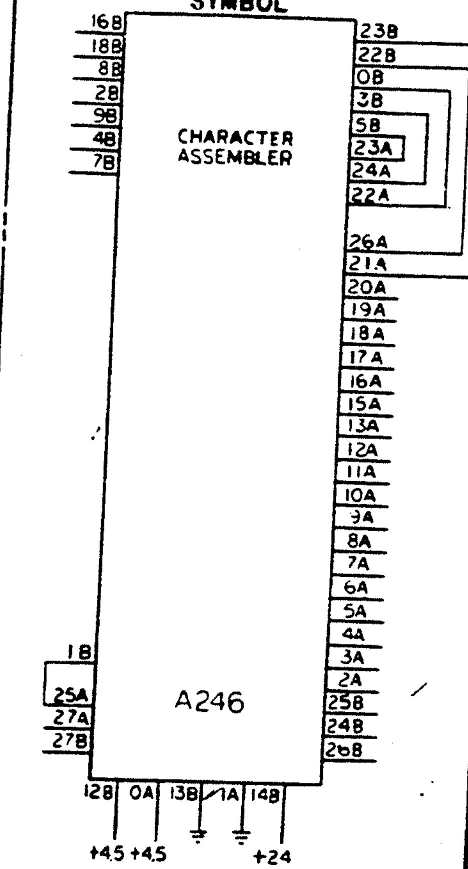
TERM.	V	I
0A	+4.5	1MA
12B	+4.5	11MA
14B	+24	63MA



SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT PACK CODE REQUIREMENTS		A246
PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		905A OR 905B
SERIES NO IDENT.	FOR LATEST CLASS "A" CHANGE	1
	FOR CURRENT MANUFACTURE	2

SYMBOL



DESCRIPTION

THIS PACKAGE CONSISTS OF TWO MECHANICALLY CONNECTED PRINTED WIRE BOARDS DESIGNATED A AND A. WHEN VIEWED FROM THE EQUIPMENT SIDE, A IS ON THE RIGHT. THE CIRCUIT IS USED TO ASSEMBLE 8 BIT SERIAL CHARACTERS INTO PARALLEL FORM AT BIT RATES OF UP TO 2400 BPS. THE CIRCUIT ALSO DETECTS THE PRESENCE OF ANY OF THE FOLLOWING THREE CHARACTERS:

BIT NO. (IN ORDER OF OCCURRENCE) 12345678
00101101 (SI)
00001011 (ENQ)
00101111 (ETB)

WHEN PROPERLY ENABLED, THE CIRCUIT ADDS A "ONE" IN THE 9TH BIT POSITION AND WRITES THE CHARACTER DIRECTLY INTO THE CORES OF THE 10A MEMORY.

INPUT SERIAL DATA IS APPLIED TO TERM 7B. ALTERNATE PULSES ON TERMS 8B AND 9B SHIFT THE INFORMATION DOWN THE REGISTER. WHEN TERM 18B IS ENABLED BY A POSITIVE PULSE (> 160 USEC), THE NEXT SHIFT PULSE ON TERM 9B GATES THE DATA IN THE FORM OF APPROXIMATELY 400 MA PULSES ONTO THE OUTPUT TERMINALS AS FOLLOWS:

DATA BIT NO. (IN ORDER OF OCCURRENCE)	1	2	3	4	5	6	7	8	9
POSITIVE	2A	4A	6A	8A	10A	12A	15A	17A	19A
NEGATIVE	3A	5A	7A	9A	11A	13A	16A	18A	20A

TERMS 2B AND 4B MUST BE ALTERNATELY PULSED TO GROUND (>160 USEC) IN ORDER TO DISCHARGE C1, C2 AND C3. A DC PRIME CURRENT OF 125 MA IS REQUIRED ON TERM 16B.

PULSES ARE APPLIED TO TERMINALS 27A AND 27B TO GATE THE CHARACTER DETECTORS. A NEGATIVE LLL OUTPUT PULSE OCCURS ON TERMS 24B, 25B AND 26B IF THE PROPER CHARACTERS ARE DETECTED. EXTERNAL STRAPPING AS SHOWN IS REQUIRED FOR CIRCUIT OPERATION.

NOTES:

1. HORIZONTAL MOUNTING CENTER 0.8 INCH.
2. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS.
INDUCTANCE VALUES ARE IN MICROHENRIES.
VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.

ISSUE 90D1

CPS A246

CIRCUIT PACK SCHEMATICS 2

SD-1A102-01-B246

BELL TELEPHONE LABORATORIES INCORPORATED

CPS A260

MF VARIOLOSSER AND GUARD DRIVER

APPARATUS LIST

CAPACITOR

DESIG	CODE
C1	602C
C2	602C
C3	535AB
C4	535AB
C5	601A
C6 (YK, YL, YR)	SEE TABLE A
C7	600A
C8	600A
C9	600A

DIODE

DESIG	CODE
CR1	~~2186A~~ 533G
CR2	~~2186A~~ 533G
CR3 J	~~2186C~~ 808E
CR4 J	~~2186D~~ 808J
CR5	~~2186A 256A~~ 533G
CR6	~~2186A 256A~~ 533G
CR7	~~2186A 256A~~ 533G
CR8	~~2186A 256A~~ 533G
CR9 J	~~2186A~~ 808B
CR10	~~2186A 256A~~ 533G
CR11 J	~~2186A~~ 808B

RESISTOR

DESIG	CODE
R1	~~2374~~, KS-20616 L1A, 898
R2	, 8250
R3	, 8250
R4	, 12.1KΩ
R5	, 12.1KΩ
R6	, 21.5KΩ
R7	, 23.7KΩ
R8	, 3620
R9	, 21.5KΩ
R10	, 4640
R11	, 8250
R12	, 31.6
R13	~~2374~~, KS-20616 L1A, 5620
R14	~~2045~~, 263A, 2.87 MΩ
R15	~~KS-19296 L40, 3830~~ KS-20239 L40, 3830
R16	~~2394~~, KS-20616 L1A, 21.5KΩ
R17	~~2394~~, KS-20616 L1A, 17.8KΩ
R18	~~2214~~, KS-20810 L1A, 5110
R19	~~2394~~, KS-20616 L1A, 10KΩ
R20	~~2394~~, KS-20616 L1A, 562
R21	~~2394~~, KS-20616 L1A, 1960
R22	~~2214~~, KS-20810 L1A, 5110

TRANSFORMER

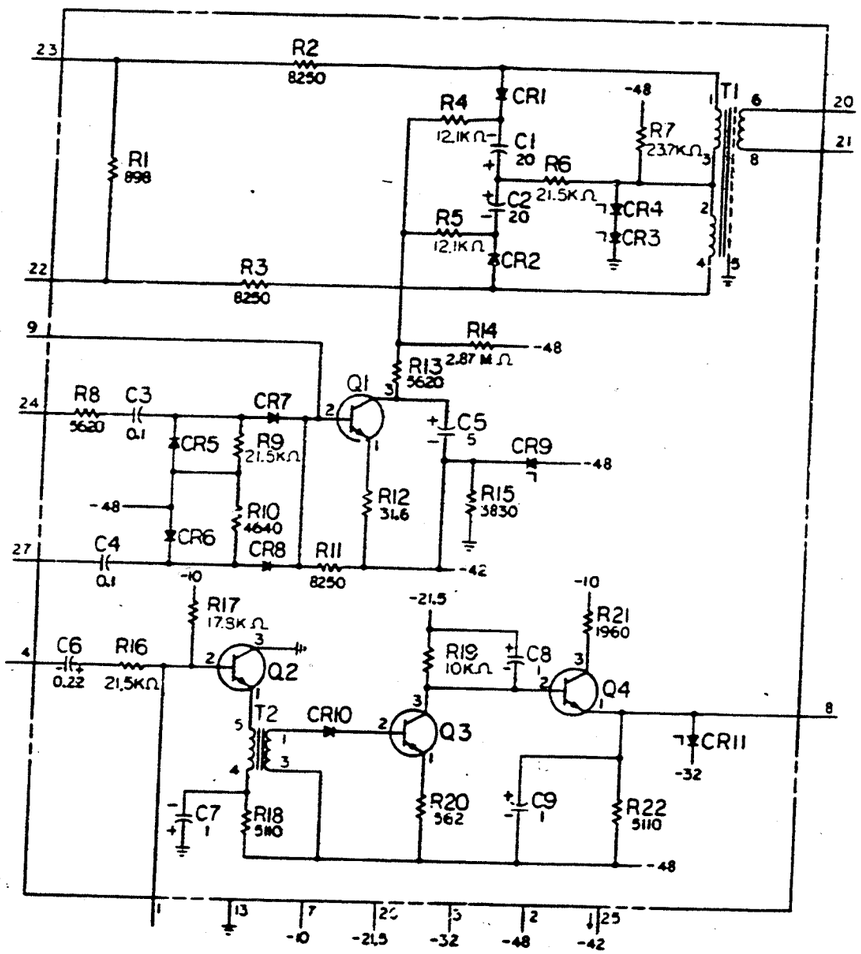
DESIG	CODE
T1	25b4AD
T2	2532H

TRANSISTOR

DESIG	CODE
Q1	~~294~~ 665
Q2	~~294~~ 665
Q3	~~294~~ 665
Q4	~~294~~ 665

TABLE A

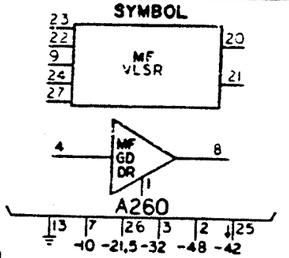
DESIG	(YK)	(YL)		(YR)
	KEMET CO	DICKSON	SPRAGUE	WE CO
	CODE	CODE	CODE	CODE
C6	KR22J60,0.22	DR22A60MU,0.22	150D224X0060A0,0.22	6078



SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT PACK CODE REQUIREMENTS		A260 A-959309
PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		305A OR 305B
SERIES NO. IDENT.	FOR LATEST CLASS "A" CHANGE	1
	FOR CURRENT MANUFACTURE	3

SYMBOL



DESCRIPTION

THIS PRINTED WIRING BOARD, INTENDED FOR USE IN A MULTI-FREQUENCY SIGNALING RECEIVER, CONTAINS TWO SEPARATE CIRCUITS: THE VARIOLOSSER WITH ITS CONTROL EQUIPMENT AND THE GUARD DRIVER AMPLIFIER.

PURPOSE: THE VARIOLOSSER PROVIDES A CONSTANT OUTPUT LEVEL FOR A WIDE RANGE OF INPUT LEVELS. THE GUARD DRIVER DEVELOPS A BIAS VOLTAGE TO PREVENT OPERATION OF MF DIGIT OUTPUTS WHEN OTHER THAN THE MF SIGNALING FREQUENCIES ARE PRESENT IN AN MF RECEIVER.

INPUTS AND OUTPUTS: THE VARIOLOSSER RECEIVES VOICE-FREQUENCY MF SIGNALS BETWEEN TERMINALS 22 AND 23 AT A LEVEL BETWEEN -2 AND -22 DBM. THE OUTPUT SIGNAL BETWEEN TERMINALS 20 AND 21 IS HELD TO ABOUT 20 MILLI-VOLTS RMS BY VARIOLOSSER ACTION. THE VARIOLOSSER IS CONTROLLED BY AN AC FEEDBACK SIGNAL OF ABOUT 8 VOLTS RMS EFFECTIVELY CENTER TAPPED TO GROUND FROM CPS A261, THE SIGNAL ENTERS A260 AT TERMINALS 24 AND 27. AN INHIBIT SIGNAL, A TIMED SHORT-CIRCUIT APPLIED BETWEEN TERMINALS 9 AND 25, PREVENTS TRANSIENTS FROM THE REVERSE-BATTERY START-PULSING SIGNAL FROM AFFECTING THE VARIOLOSSER AND THE FOLLOWING CIRCUITRY. THE GUARD DRIVER RECEIVES AN INPUT VOICE FREQUENCY SIGNAL OF ABOUT 5 VOLTS RMS AT TERMINAL 4. MF SIGNALING FREQUENCIES ARE SHORTED OUT BY SERIES RESONANT TUNED CIRCUITS CONNECTED TO GROUND AT TERMINAL 1. ANY REMAINING VOICE FREQUENCY ENERGY IS RECTIFIED, AMPLIFIED, AND MADE AVAILABLE AT TERMINAL 8. THIS "GUARD VOLTAGE" IS CLAMPED TO ABOUT -32 VOLTS RELATIVE TO GROUND WHEN NO VOICE FREQUENCY ENERGY IS PRESENT, AND TO ABOUT -38 VOLTS WHEN NON-MF VOICE FREQUENCY SIGNALS OCCUR.

OPERATION: THE VARIOLOSSER CONSISTS OF A PAD WITH ONE OF ITS TWO SHUNT ARMS VARIABLE. CR1 AND CR2 HAVE A HIGH AC IMPEDANCE WHEN A SMALL DC CURRENT FLOWS THROUGH THEM, AND A MUCH LOWER AC IMPEDANCE WHEN THE DC INCREASES. DC IS APPLIED BY Q1, UNDER CONTROL OF THE OUTPUT OF THE FULL-WAVE VOLTAGE DOUBLER RECTIFIER COMPOSED OF CR5, CR6, CR7, AND CR8 AND THE ASSOCIATED CIRCUITRY. THE RECTIFIER'S INPUT IS OBTAINED FROM A VOICE FREQUENCY SIGNAL WHOSE LEVEL IS PROPORTIONAL TO THE VARIOLOSSER OUTPUT. THE GUARD DRIVER IS AN AC AMPLIFIER, Q2, FOLLOWED BY A POWER RECTIFIER, Q3. THE FILTERED OUTPUT OF Q3 IS DECOUPLED BY THE EMITTER-FOLLOWER TRANSISTOR Q4.

NOTES:

1. HORIZONTAL MOUNTING CENTER 1.6 INCH.
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS.
   CAPACITANCE VALUES ARE IN MICROFARADS.
   VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.

DRAWING ISSUE

244	JS
250	JS
380	JS
560	JS

REPLACES SD-1A102-01-8149

CPS A260

ISSUE 95D

CIRCUIT PACK SCHEMATICS (2) SD-1A102-01-B260

AT&T BELL LABORATORIES 65

SD-1A102-01-B260

CPS A261
MF AGC AMPLIFIER AND SIGNAL DRIVER

APPARATUS LIST

CAPACITOR

DESIG	CODE
C1	5700F, 681PF
C2	602B
C3	601A
C4	601A
C5	535AD
C6	570CA
C7	~~808A~~ 614A
C8	570GB

DIODE

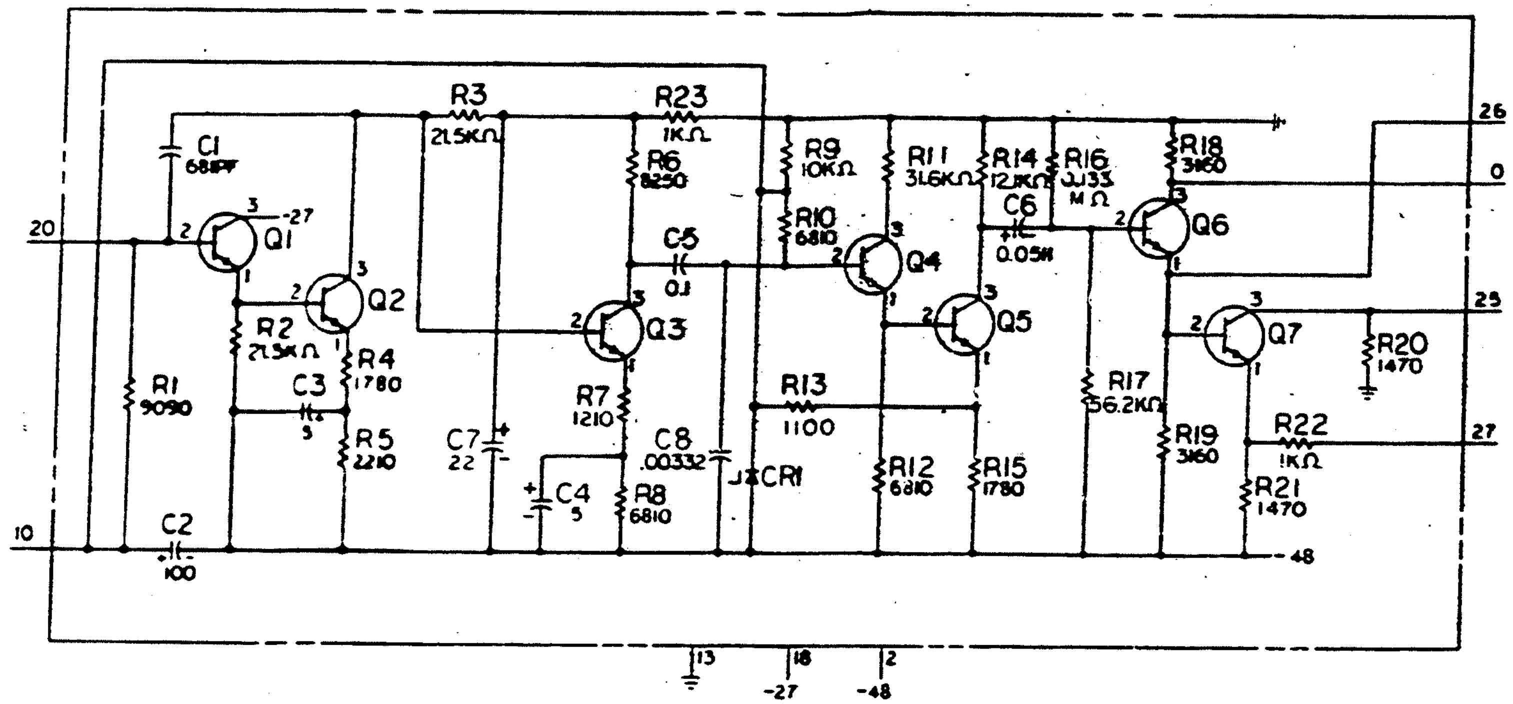
DESIG	CODE
CR1	~~[illegible]~~ 8088

RESISTOR

DESIG	CODE
R1	239A KS-20616 L1A, 9090
R2	↓ ↓ ,21.9KΩ
R3	,21.9KΩ
R4	,1780
R5	.2210
R6	,8250
R7	,1210
R8	239A KS-20616 L1A, 5810
R9	221A KS-20810 L1A, 10KΩ
R10	239A KS-20616 L1A, 6810
R11	↓ ↓ ,51.6KΩ
R12	,6810
R13	,1100
R14	,12.1KΩ
R15	,1780
R16	,0.133 MΩ
R17	~~237A~~ KS-20616 L1A, 56.2KΩ
R18	~~221A, 3160~~ KS-20810 L1A, 3160
R19	~~221A, 3160~~ KS-20810 L1A, 3150
R20	~~221A, 1470~~ KS-20810 L1A, 1470
R21	~~281A 1470~~ KS-20810 L1A, 1470
R22	~~237A, 1K~~ KS-20616 L1A, 1KΩ
R23	~~237A, 1K~~ KS-20616 L1A, 1KΩ

TRANSISTOR

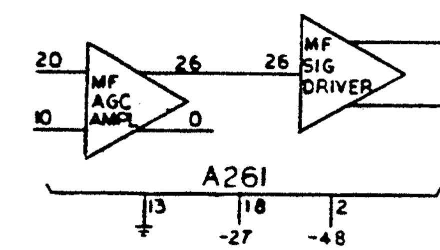
DESIG	CODE
Q1	29A 66S
Q2	↓ ↓
Q3	
Q4	
Q5	
Q6	29A 66S
Q7	~~200 OR 201~~ 139A



SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT PACK CODE REQUIREMENTS PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		A261 A-858310 905A OR 905B
SERIES NO. IDENT.	FOR LATEST CLASS "A" CHANGE	3
	FOR CURRENT MANUFACTURE	5

SYMBOL



DESCRIPTION

THE AGC AMPLIFIER TAKES THE RELATIVELY CONSTANT OUTPUT FROM THE VARIOLOSSER AND AMPLIFIES IT TO SUCH A LEVEL THAT IT CAN BE APPLIED TO THE SIGNAL AND GUARD DRIVERS. A SUITABLE OUTPUT IS ALSO DEVELOPED TO DRIVE THE FULL WAVE RECTIFIER WHICH IS PART OF THE MF VARIOLOSSER CIRCUIT ON A260. TRANSISTORS Q2, Q3, AND Q5 FORM A CASCADE OF THREE CLASS A COMMON-EMITTER AMPLIFIER STAGES WITH EMITTER DEGENERATION SUPPLIED BY RESISTORS R4, R7, R13, AND R15. EMITTERS Q1 AND Q4 MINIMIZE VARIATIONS IN INPUT AND INTERSTAGE IMPEDANCES RESPECTIVELY. Q6 ACTS AS BOTH AN EMITTER FOLLOWER OUTPUT AMPLIFIER AND A PHASE INVERTER FOR THE VARIOLOSSER FULL-WAVE RECTIFIER. THE AGC AMPLIFIER RECEIVES A VOICE-FREQUENCY INPUT SIGNAL FROM THE MF VARIOLOSSER BETWEEN TERMINALS 10 AND 20, AND DRIVES THE MF GUARD DRIVER WITH A SIGNAL FROM TERMINAL 26 . A FEED-BACK SIGNAL IS ALSO APPLIED TO THE VARIOLOSSER FROM TERMINALS 0 AND 26. THE MF VARIOLOSSER AND GUARD DRIVER ARE BOTH ON CIRCUIT PACK A260. THE AGC AMPLIFIER ALSO DRIVES THE MF SIGNAL DRIVER, PART OF A261.

THE MF SIGNAL AMPLIFIER, Q7, DRIVES THE FREQUENCY-SELECTING TUNED CIRCUITS ON A264 AND A265. R22, BETWEEN Q7 AND OUTPUT TERMINAL 27, MODIFIES THE RESPONSE OF THE TUNED CIRCUITS. THE OUTPUT DEVELOPED ACROSS R20 AND AVAILABLE AT TERMINAL 25 STARTS THE MF SP TIMER, CIRCUIT PACK A266.

NOTES:

1. HORIZONTAL MOUNTING CENTER 0.8 INCH.
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS.
   CAPACITANCE VALUES ARE IN MICROFARADS.
   VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.

REPLACES SD-1A102-01-B150

CPS A261

ISSUE 95D

CIRCUIT PACK SCHEMATICS

SD-1A102-01-B261

AT&T BELL LABORATORIES

8S

SD-1A102-01-B261

APPARATUS LIST

CAPACITOR

DESIG		CODE		
(XP)	C1	~~542Y0~~ 594G		
(XN,XA)	C1	(WN) KS-16591 L2,8250	(WP)	KS-16591 L27, 8250
(XN,XB)	C1	KS-13368 L11,8250		
(XN)	C2	(WN) KS-14056 L11,383	(WP)	KS-14056 L27, 383
(XN)	C3	KS-13367 L13,5110		KS-13367 L27, 5110
(XN)	C4	KS-14056 L11,100		KS-14056 L27, 100
(XN)	C5	KS-13367 L13,3320		KS-13367 L27, 3320
(XN)	C6	(WN) KS-14056 L11,180	(WP)	KS-14056 L27, 180
(XN)	C7	542Y0		
(XP)	CA	570JF		
(XP)	CB	570JT		
(XP)	CC	570NN		

INDUCTOR

DESIG	CODE
L1	1631W
L2	1631W
L3	1631W

RESISTOR

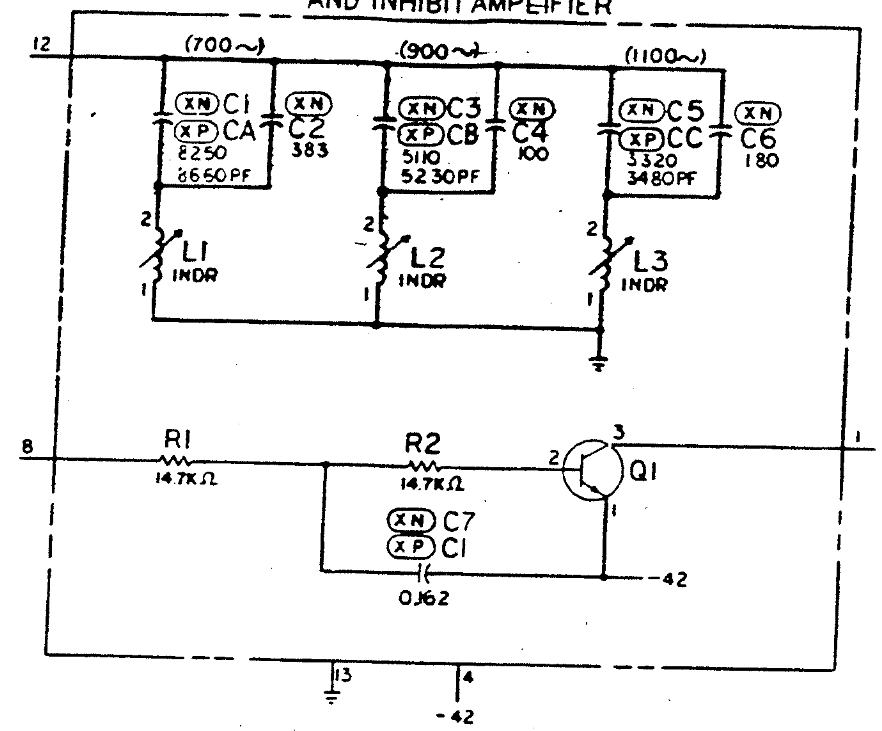
DESIG	CODE
R1	~~297A, 14.2K~~ KS-20616 L1A, 14.7KΩ
R2	~~297A, 14.2K~~ KS-20616 L1A, 14.7KΩ

TRANSISTOR

DESIG	CODE
Q1	29A

CPS A262

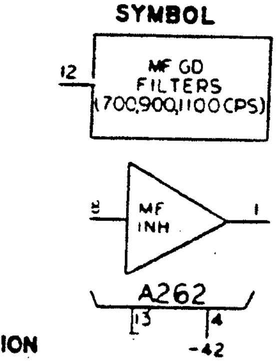
MF GUARD FILTERS (700,900,1100 CPS) AND INHIBIT AMPLIFIER



SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT PACK CODE REQUIREMENTS PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		A262 A-858313 905A OR 905B
SERIES NO.	FOR LATEST CLASS "A" CHANGE	1
IDENT.	FOR CURRENT MANUFACTURE	2

SYMBOL



DESCRIPTION

THIS PRINTED WIRE BOARD CONTAINS THREE SERIES-TUNED LC CIRCUITS, EACH RESONANT TO ONE OF THE MF SIGNALING FREQUENCIES. WHEN CONNECTED IN PARALLEL WITH CIRCUIT PACK A263, LOW IMPEDANCE TO GROUND IS PROVIDED CLOSE TO ALL SIX OF THE MF SIGNALING FREQUENCIES, WITH HIGH IMPEDANCE TO GROUND ELSEWHERE IN THE VOICE FREQUENCY BAND. A262 AND A263 ARE DESIGNED TO SHORT SIGNALING FREQUENCIES OUT OF THE MF GUARD DRIVER ON CIRCUIT PACK A260; THUS THE MF GUARD DRIVER IS ABLE TO PRODUCE A DC BIAS VOLTAGE PROPORTIONAL TO ALL VOICE FREQUENCIES REACHING IT EXCLUSIVE OF MF SIGNALING FREQUENCIES.

THE MF INHIBIT AMPLIFIER, Q1 AND ITS ASSOCIATED COMPONENTS, BLOCKS TRANSIENTS FROM THE MF VARIOLOSSER CONTROL AMPLIFIER ON A260 FOR ABOUT 20 MSEC AFTER THE MF RECEIVER SENDS A REVERSE-BATTERY START-PULSING SIGNAL. UNTIL THIS SIGNAL IS SENT, INPUT TERMINAL 8 IS CONNECTED TO GROUND AND TRANSISTOR Q1 IS SATURATED BETWEEN OUTPUT TERMINAL 1 AND -42 VOLTS ON TERMINAL 4 . TERMINALS 1 AND 4 ARE ACROSS THE INPUT OF THE VARIOLOSSER CONTROL TRANSISTOR ON A260, AND, WHEN Q1 IS SATURATED, THE VARIOLOSSER CONTROL INPUT IS SHORTED. C1 DISCHARGES THROUGH R2 AND Q1 FOR ABOUT 20 MSEC AFTER THE START PULSING SIGNAL IS SENT AND INPUT 8 IS DISCONNECTED FROM GROUND. WHEN Q1 CEASES TO CONDUCT, THE CONTROL TRANSISTOR IN THE MF VARIOLOSSER CAN OPERATE PROPERLY. THIS SEQUENCE OF EVENTS PREVENTS THE LARGE REVERSE-BATTERY START-PULSING TRANSIENT ON THE TRUNK FROM BLOCKING THE VARIOLOSSER FOR A PROLONGED PERIOD OF TIME.

NOTES:

1. HORIZONTAL MOUNTING CENTER 1.6 INCH.
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL + (PLUS) OR − (MINUS) ARE IN VOLTS.

CPS A262

ISSUE 9OD1

CIRCUIT PACK SCHEMATICS

SD-1A102-01-B262

BELL TELEPHONE LABORATORIES INCORPORATED | 6S

SD-1A102-01-B262

CPS A263
MF GUARD FILTERS
(1300,1500,1700 CPS)

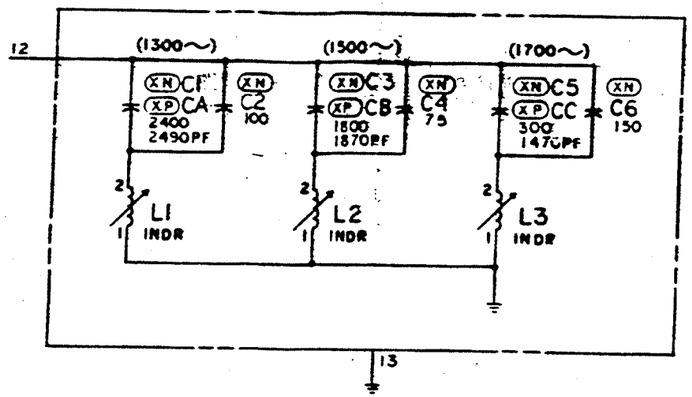
APPARATUS LIST

CAPACITOR

DESIG	CODE				
XN C1	XN	KS-13367 L13,2400	XP	KS-13367 L27, 2400
C2		KS-14056 L11,100		KS-14056 L27, 100
C3		KS-13367 L13,1800		KS-13367 L27, 1800
C4		KS-14056 L11,75		KS-14056 L27, 75
C5		KS-13367 L13,1300		KS-13367 L27, 1300
XN C6	XN	KS-14056 L11,150	XP	KS-14056 L27, 150
XP CA		570 NG		
XP CB		570 ND		
XP CC		570 EY		

INDUCTOR

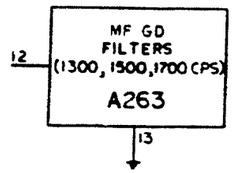
DESIG	CODE
L1	1631M
L2	1631M
L3	1631M



SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT PACK CODE REQUIREMENTS PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		A263 A-858313 905A OR 905B
SERIES NO. IDENT.	FOR LATEST CLASS "A" CHANGE	1
	FOR CURRENT MANUFACTURE	2

SYMBOL



DESCRIPTION

THIS PRINTED WIRE BOARD CONTAINS THREE SERIES-TUNED LC CIRCUITS, EACH RESONANT TO ONE OF THE MF SIGNALING FREQUENCIES. WHEN CONNECTED IN PARALLEL WITH CIRCUIT PACK A262, LOW IMPEDANCE TO GROUND IS PROVIDED CLOSE TO ALL SIX OF THE MF SIGNALING FREQUENCIES, WITH HIGH IMPEDANCE TO GROUND ELSEWHERE IN THE VOICE FREQUENCY BAND. A262 AND A263 ARE DESIGNED TO SHORT SIGNALING FREQUENCIES OUT OF THE MF GUARD DRIVER ON CIRCUIT PACK A260; THUS THE MF GUARD DRIVER IS ABLE TO PRODUCE A DC BIAS VOLTAGE PROPORTIONAL TO ALL VOICE FREQUENCIES REACHING IT EXCLUSIVE OF MF SIGNALING FREQUENCIES.

NOTES:
1. HORIZONTAL MOUNTING CENTER 1.6 INCH.
2. UNLESS OTHERWISE SPECIFIED:
   CAPACITANCE VALUES ARE IN MICROFARADS.

DRAWING ISSUE

24A	
23D	
56D	
59D	

ISSUE 8101

CIRCUIT PACK SCHEMATICS (2) SD-1A102-01-B263

BELL TELEPHONE LABORATORIES INCORPORATED 6S

SD-1A102-01-B263

APPARATUS LIST

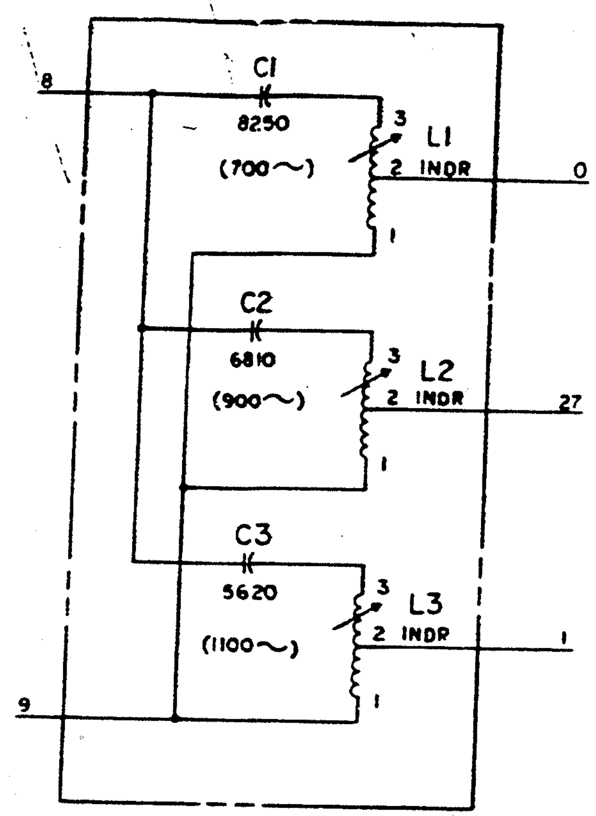
CAPACITOR

DESIG	CODE
C1	(XN) KS-16591 L2, 8250 (XP) 570CR OR KS-16591 L27, 8250
C2	(XN) KS-16591 L2, 6810 (XP) 570JJ OR KS-16591 L27, 6810
C3	(XN) KS-13367 L13, 5620 (XP) 570JR OR KS-13367 L27, 5620

INDUCTOR

DESIG	CODE
L1	1631N
L2	1631P
L3	1631R

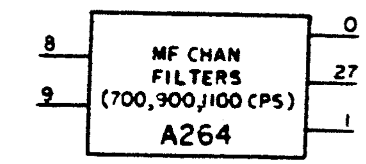
CPS A264
CHANNEL FILTERS
(700,900,1100 CPS)



SUPPORTING INFORMATION

CATETORY		NO.
CIRCUIT PACK CODE REQUIREMENTS PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		A264 A-858313 905A OR 905B
SERIES NO. IDENT.	FOR LATEST CLASS "A" CHANGE	1
	FOR CURRENT MANUFACTURE	1

SYMBOL



DESCRIPTION

THIS PRINTED WIRE BOARD CONTAINS THREE SERIES-TUNED LC CIRCUITS, EACH RESONANT TO ONE OF THE MF SIGNALING FREQUENCIES. EACH INDUCTOR IS TAPPED TO PROVIDE PROPER DRIVE TO THE MF CHANNEL DETECTORS ON CIRCUIT PACK A152. INPUT TERMINALS 8 AND 9 ARE DRIVEN IN PARALLEL WITH THOSE OF CIRCUIT PACK A265; THE SIX INDIVIDUAL OUTPUT LEADS AT TERMINALS 0, 27, AND 1 ON THE TWO BOARDS RESPOND ONLY TO THE MF SIGNALING FREQUENCIES AND PROVIDE SUITABLY ISOLATED OUTPUT SIGNALS.

NOTES:

1. HORIZONTAL MOUNTING CENTER 1.6 INCH.
2. UNLESS OTHERWISE SPECIFIED:
   CAPACITANCE VALUES ARE IN PICOFARADS.

DRAWING ISSUE: 24A, 25D, 56D, 59D

ISSUE 81D1

CIRCUIT PACK SCHEMATICS

BELL TELEPHONE LABORATORIES

SD-1A102-01-B264

SD-1A102-01-B264

APPARATUS LIST

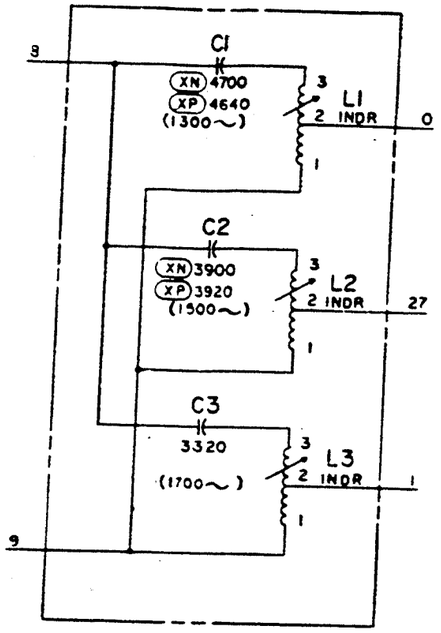
CAPACITOR

DESIG	CODE
C1	(XN) KS-13367 L13,4700 (XP) 570JU OR KS-13367 L27, 4700
C2	(XN) KS-13367 L13,3920 (XP) 570LK OR KS-13367 L27, 3920
C3	(XN) KS-13367 L13,3320 (XP) 570MM OR KS-13367 L27, 3320

INDUCTOR

DESIG	CODE
L1	1631S
L2	1631T
L3	1631U

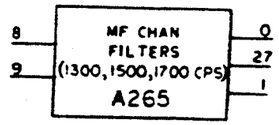
CPS A265
CHANNEL FILTERS
(1300,1500,1700 CPS)



SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT PACK CODE REQUIREMENTS PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		A265 A-858313 905A OR 905B
SERIES NO. IDENT.	FOR LATEST CLASS "A" CHANGE	1
	FOR CURRENT MANUFACTURE	2

SYMBOL



DESCRIPTION

THIS PRINTED WIRE BOARD CONTAINS THREE SERIES-TUNED LC CIRCUITS, EACH RESONANT TO ONE OF THE MF SIGNALING FREQUENCIES. EACH INDUCTOR IS TAPPED TO PROVIDE PROPER DRIVE TO THE MF CHANNEL DETECTORS ON CIRCUIT PACK A152. INPUT TERMINALS 8 AND 9 ARE DRIVEN IN PARALLEL WITH THOSE OF CIRCUIT PACK A264; THE SIX INDIVIDUAL OUTPUT LEADS AT TERMINALS 0, 27, AND 1 ON THE TWO BOARDS RESPOND ONLY TO THE MF SIGNALING FREQUENCIES AND PROVIDE SUITABLY ISOLATED OUTPUT SIGNALS.

NOTES:
1. HORIZONTAL MOUNTING CENTER 1.6 INCH.
2. UNLESS OTHERWISE SPECIFIED: CAPACITANCE VALUES ARE IN PICOFARADS.

DRAWING ISSUE
24A
25D
26D
59D

ISSUE 8 1D1

CIRCUIT PACK SCHEMATICS (2) SD-1A102-01-B265

BELL TELEPHONE LABORATORIES INCORPORATED 65

SD-1A102-01-B265

CPS A266

MF SP TIMER

APPARATUS LIST

CAPACITOR

DESIG	CODE
C1	542A
C2	535G
C3	542AD
C4	600A
C5	535G

DIODE

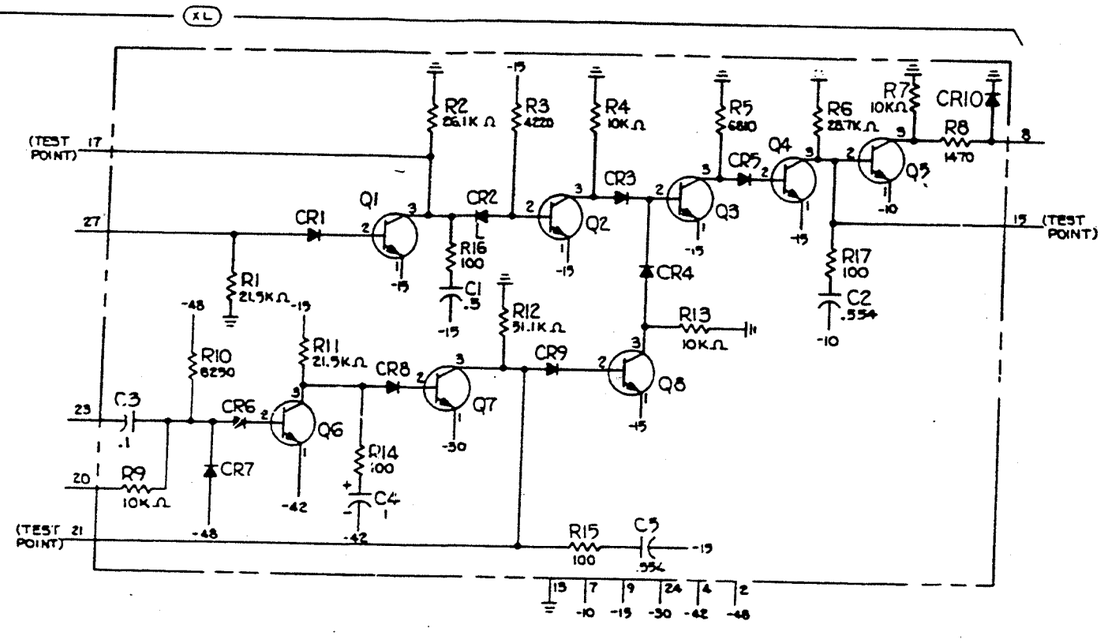
DESIG	CODE
CR1	(ZZ) 458C, (ZY) 447A
CR2	446B
CR3	(ZZ) 458C, (ZY) 447A
CR4	
CR5	
CR6	
CR7	
CR8	
CR9	
CR10	(ZZ) 458C, (ZY) 447A

RESISTOR

DESIG	CODE
R1	237A, 21.5KΩ
R2	237A, 26.1KΩ
R3	237A, 4220
R4	237A, 10KΩ
R5	237A, 6810
R6	237A, 28.7KΩ
R7	237A, 10KΩ
R8	221A, 1470
R9	237A, 10KΩ
R10	237A, 8250
R11	237A, 21.5KΩ
R12	237A, 51.1KΩ
R13	237A, 10KΩ
R14	KS-19150 L2, 100
R15	KS-19150 L2, 100
R16	KS-19150 L2, 100
R17	KS-19150 L2, 100

TRANSISTOR

DESIG	CODE
Q1	294
Q2	
Q3	
Q4	
Q5	
Q6	
Q7	
Q8	294



APPARATUS LIST

CAPACITOR

DESIG	CODE
C1	701G, .619
C2	701C, .511
C3	~~53288-7228~~ 702G
C4	535JJ
C5	701C, .511
C6	594G, .0196
C7	594G, .147

DIODE

DESIG	CODE
CR1	458C
CR2	458C
CR3	~~446A~~ 308E
CR4	458C
CR5	
CR6	
CR7	
CR8	
CR9	
CR10	
CR11	
CR12	
CR13	458C

RESISTOR

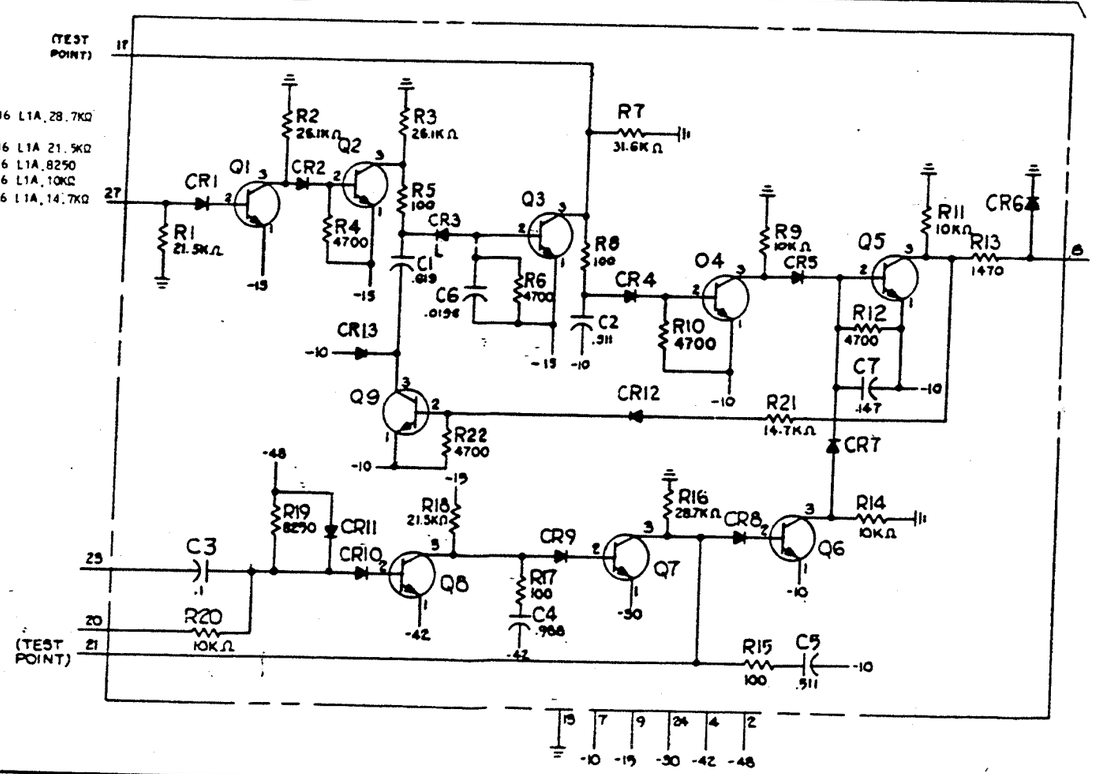
DESIG	CODE
R1	~~2378, 21.5K~~ KS-20616 L1A, 21.5KΩ
R2	~~2378, 26.1K~~ KS-20616 L1A, 26.1KΩ
R3	~~2378, 26.1K~~ KS-20616 L1A, 26.1KΩ
R4	KS-19150 L2, 4700
R5	KS-19150 L2, 100
R6	KS-19150 L2, 4700
R7	~~2378, 31.6K~~ KS-20616 L1A, 31.6KΩ
R8	KS-19150 L2, 100
R9	~~2378, 10K~~ KS-20616 L1A, 10KΩ
R10	KS-19150 L2, 4700
R11	~~2378, 10K~~ KS-20616 L1A, 10KΩ
R12	KS-19150 L2, 4700
R13	~~2378, 1470~~ KS-20616 L1A, 1470
R14	~~2378, 10K~~ KS-20616 L1A, 10KΩ

RESISTOR (CONT)

DESIG	CODE
R15	KS-19150 L2, 100
R16	~~2378, 28.7K~~ KS-20616 L1A, 28.7KΩ
R17	KS-19150 L2, 100
R18	~~2378, 21.5K~~ KS-20616 L1A 21.5KΩ
R19	~~2378, 8250~~ KS-20616 L1A, 8250
R20	~~2378, 10K~~ KS-20616 L1A, 10KΩ
R21	~~2378, 14.7K~~ KS-20616 L1A, 14.7KΩ
R22	KS-19150 L2, 4700

TRANSISTOR

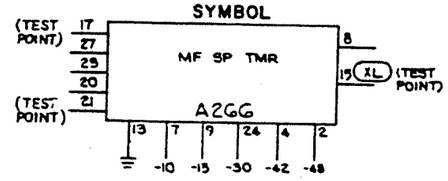
DESIG	CODE
Q1	294
Q2	
Q3	
Q4	
Q5	
Q6	
Q7	
Q8	
Q9	294



SUPPORTING INFORMATION

CATEGORY		NO.
CIRCUIT PACK CODE REQUIREMENTS PLUG-IN CONNECTOR ON FRAME (RECEPTACLE)		A266 A-858314 905A OR 905B
SERIES NO. IDENT.	FOR LATEST CLASS "A" CHANGE	4
	FOR CURRENT MANUFACTURE	4

SYMBOL



DESCRIPTION

PURPOSE: THE MF SIGNAL PRESENT TIMER PREVENTS VOICE FREQUENCY SIGNALS FROM SIMULATING MF DIGITS BY (1) TIMING THE OUTPUT OF THE MF SIGNAL AMPLIFIER ON A261 WHEN THAT OUTPUT IS ABOVE A THRESHOLD LEVEL AND (2) BY TIMING THE PRESENCE OF TWO (OR MORE) ACTIVE OUTPUTS FROM THE A152 CHANNEL DETECTORS. IF THESE OUTPUTS PERSIST FOR LONGER THAN 20 AND 10 MS RESPECTIVELY, THE PROBABILITY THAT THEY REPRESENT A VALID SIGNAL IS HIGH. IF THEY TERMINATE EARLY, THE TIMERS ARE RESET BEFORE AN OUTPUT INDICATION IS GIVEN. THE MF SIGNAL PRESENT TIMER ALSO PREVENTS DOUBLE REGISTRATION OF VALID MF DIGITS WHICH MAY BE INTERRUPTED BY NOISE SIGNALS. ONCE THE OUTPUT BECOMES ACTIVE, INPUT SIGNALS MUST BE ABSENT FOR 20 MS BEFORE THE OUTPUT WILL RETURN TO THE INACTIVE STATE.

INPUTS AND OUTPUTS: EACH ACTIVE OUTPUT ON AN MF CHANNEL DETECTOR (A152) CONNECTS THE SP TIMER INPUT TERMINAL 27 TO -27 VOLTS THROUGH A RESISTOR. TWO OR MORE CHANNEL DETECTORS ACTIVE WILL PULL TERMINAL 27 BELOW -15 VOLTS TO START THE 10 MS 2 OUT OF 6 TIMER. THE DC INPUT AT TERMINAL 23 IS DRIVEN IN PARALLEL WITH THE SIGNAL DRIVER ON A261 AND THE VARIOLOSSER CONTROL AMPLIFIER ON A260. WHEN THIS SIGNAL IS APPROXIMATELY EQUAL TO OR LARGER THAN THAT NECESSARY TO START AGC ACTION IN THE VARIOLOSSER, THE 20 MS DC SIGNAL TIMER IS STARTED. THE INPUT AT TERMINAL 20 PERMITS THE AC SIGNAL TIMER TO BE STARTED BY A DC SIGNAL IN A TEST STATE. THE OUTPUT AT TERMINAL 8 WILL DRAW ABOUT 6 MA FROM GROUND THROUGH A FERROD SENSOR IN THE SCANNER. WHEN NO SP INDICATION IS TO BE GIVEN (0 OUTPUT) AND NO CURRENT (1 OUTPUT) FOR SIGNAL PRESENT.

OPERATION: THE 2 OUT OF 6 TIMER IS STARTED WHEN INPUT TERMINAL 27 GOES BELOW -15 VOLTS. TRANSISTOR Q1 CUTS OFF PERMITTING C1 TO CHARGE TO THE REVERSE BREAKDOWN VOLTAGE OF CR2 (ABOUT 6 VOLTS). WHEN CR2 CONDUCTS, Q2 SATURATES TO MAKE ONE INPUT TO AN AND GATE ACTIVE. THE AC SIGNAL TIMER IS STARTED WHEN THE RECTIFIED SIGNAL FROM TERMINAL 23 CAUSES Q6 TO CONDUCT WHICH IN TURN CUTS OFF Q7. THE OUTPUT OF Q6 IS FILTERED BY R11 AND C4. WHEN Q7 CUTS OFF, C5 CHARGES VIA R12 FROM -30 TOWARD GROUND. AT ABOUT -15 VOLTS, Q8 CONDUCTS TO ENABLE THE SECOND SIDE OF THE CR3 - CR4 AND GATE. Q3, FORMERLY SATURATED, CUTS OFF TO TURN ON Q4. THIS, IN TURN, CUTS OFF Q5 AND NO CURRENT FLOWS THROUGH THE OUTPUT TERMINAL. WHEN EITHER TIMER INPUT CEASES, THAT TIMER IS RESET QUICKLY AND THE AND GATE IS DEACTIVATED. THIS TURNS ON Q3 AND TURNS OFF Q4. C2 CHARGES FROM -15 VOLTS TOWARD GROUND AND TURNS ON Q5 TO DRAW OUTPUT CURRENT AFTER THE RELEASE DELAY INTERVAL.

NOTES:

1. HORIZONTAL MOUNTING CENTER 0.8 INCH.
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS,
   CAPACITANCE VALUES ARE IN MICROFARADS,
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.

DRAWING ISSUE 588 73A

ISSUE 9401

REPLACES SD-1A102-01-B153 AND B154

CPS A266

CIRCUIT PACK SCHEMATICS (2) SD-1A102-01-B266

BELL TELEPHONE LABORATORIES INCORPORATED 6S

SD-1A102-01-B266