Just twelve basic designs are used in the hundreds of thousands of individual semiconductors in No. 1 ESS. Device designers achieved this compression by exploiting the full capabilities of each design so that it could be used in many circuit functions.

Semiconductor Devices

M. L. Embree and J. Sevick

IN 1948, BELL LABORATORIES MADE a quiet announcement to the press and started a revolution in the electronics industry. It revealed the invention of the transistor, a tiny device that together with semiconductor diodes held the germ of No. 1 ESS with its hundreds of thousands of semiconductor devices.

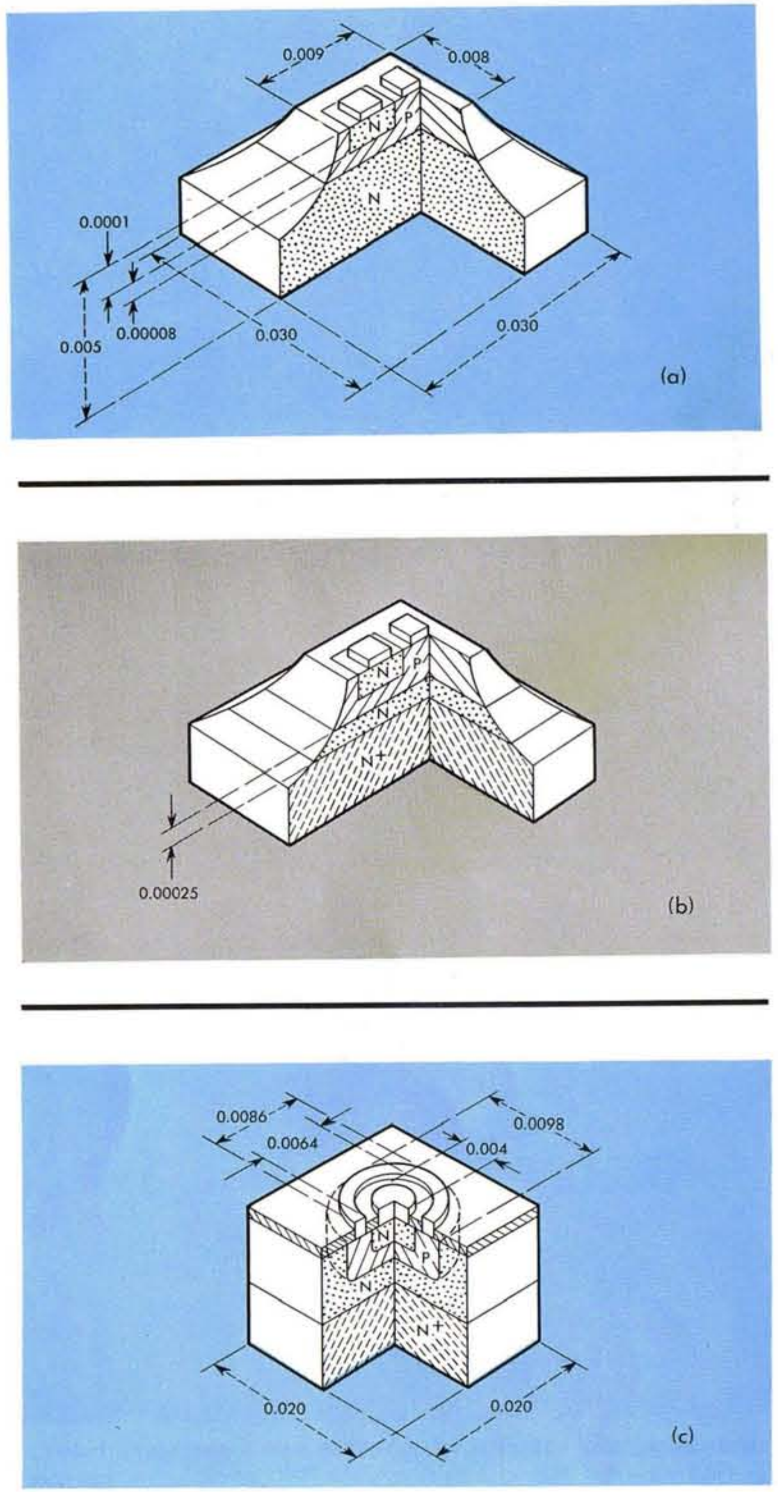
The advantages of semiconductor devices were immediately apparent. They operated at extremely low power and did not have either the hot cathodes of vacuum tubes or the mechanical parts of relays. But in 1948, the semiconductor devices were rather primitive. Between them and the semiconductor devices of No. 1 ESS lie almost two decades of intensive research and development pointing toward continually improving electrical performance, increasing reliability, and lowered costs.

By 1956 semiconductor devices were reliable enough to be used in the trial of the Morris electronic central office. And in the eight years between Morris and Succasunna, silicon devices using diffusion technology were perfected and giant steps in reliability were achieved.

By the time development started on No. 1 ESS, many types of transistors and diodes were available to the circuit designer. There was such a large number of types in fact, that indiscriminately used they could have created difficult problems in development and manufacturing. In No. 1 ESS, therefore, the trend was toward concentration—the goal was as few types of transistors and diodes as possible. Every pertinent factor, from system philosophy to device physics, was weighed in characterizing the types of semiconductor devices No. 1 ESS required. The primary objective was versatile and reliable performance at an overall minimum cost. Most of the transistors and diodes in the system are miniature switching types used primarily in logic circuits. The graph on page 267 shows the different types of devices, their functions, and the number of each type for a typical 10,000 line central office.

A diode coupled AND-NOT gate, generally known as a low-level logic (LLL) circuit, is the basic building block of No. 1 ESS. It is a high performance circuit combining fast switching speeds, large fan-in and fan-out (i.e. the number of signals that can be applied to the input of the circuit and the number it can handle as output, respectively), and excellent margin. With this approach, only three types of transistors and eight types of diodes fill the No. 1 ESS semiconductor requirements. Actually, one of the three transistors, a varistor and a reference diode, are employed in such small numbers that they do not

Miss Gloria Schirmacher of the Allentown Laboratory rinsing logic transistor slices in preparation for the diffusion process.



The evolution of the logic transistor for No. 1 ESS. The first stage (a) is a diffused base silicon mesa structure. The second (b) is an epitaxial structure. The last stage (c) is the planar epitaxial structure. The crystal substrate is designated N+ in (b) and (c).

appreciably affect the reliability or cost of the system. This article, then, will discuss only two transistors and seven diodes.

Transistors

The first transistor, designated 29A, is a logic device capable of switching in less than 50 nanoseconds. The second, the 20D, is a 1-ampere memory driver. Prototypes of these devices were first made in 1959, and their developments since then have similar stories of evolving inside structures and outside packaging. This part of the story can be told in terms of the 29A alone.

The history of the logic transistor (see the drawings on this page) begins with a diffused mesa silicon device. To reduce the storage effects of minority carriers in the base and collector regions which hampered switching speed, the wafer was quick-quenched after diffusion. Vacuum-baking was also necessary to remove moisture and this necessitated a tubulated, single-ended case. The great disadvantage of this transistor was that it could not handle the 24 volts required by No. 1 ESS.

Epitaxial transistors, announced by Bell Laboratories in 1960, solved the problem. Growing the desired silicon layer for the device on a highly conducting silicon substrate resulted in lower saturation voltages and higher breakdown voltages. The result was a more efficient switch that met the 24-volt requirement. In this second stage of its evolution, the logic transistor was packaged in a double-ended case allowing it to be placed in slots in a circuit board. This lowered profile contributed to a thinner circuit package.

A planar-epitaxial transistor, the 29A, succeeded the mesa device. These transistors retain all the advantages of mesa-epitaxial transistors and have some improved electrical parameters as well. Junction boundaries for a planar transistor are defined by completely photographic techniques and the junctions are protected by oxide formations. The process leads to devices with lower leakage currents, flatter gain characteristics, and lower base resistances and noise figures. It also contributes toward more economical fabrication and manufacture. For example, because planar wafers are more easily tested than mesa structures, data on uniformity and other important parameters are obtained before wafers are mounted, thus assuring high yields during subsequent steps where the investment is larger. Planar wafers are also less sensitive to ambient conditions than the mesa structure with its exposed junctions.

Changes in the high-current switching transistor, the 20D, follow much the same pattern of new structures leading to improved electrical performance and reliability. The forerunner of the 20D was a 30-volt 750-milliampere device that, in 1959, was the only transistor available to drive the high currents required of magnetic memories. Shortly after that, the developing requirements of No. 1 ESS created a need for a device with a sustaining voltage of 50 volts and a low saturation voltage above 1 ampere. This occurred at about the same time as the development of the epitaxial transistor, so the new demand and the way to fulfill it coincided.

The epitaxial 20D transistor has a high sustaining voltage, low saturation voltage, high current gain at 1 ampere, and relatively fast switching speeds. Its economy is realized in simpler circuits, larger circuit margins, and an ability to fulfill many amplifying functions.

Diodes

Diodes comprise the greatest number of semiconductor devices in a No. 1 ESS office. A typical 10,000 line office contains over 200,000 diodes of eight types which are used for logic switching, energy storage, voltage level shifting, memory access isolation, voltage regulation and numerous other relatively minor applications.

Diodes are electronic devices which act as good conductors when voltage of one polarity is applied and perform as good insulators for potentials of the opposite polarity. The critical junction region of the diodes used in No. 1 ESS is formed by high temperature diffusion of boron into one side and phosphorous into the other side of a thin slice of ultra pure single crystal silicon. Ohmic (non-rectifying) metallic contacts are plated on the surfaces and the slice is cut into properly sized and shaped wafers.

Over 80 per cent of the No. 1 ESS diode complement is made up of two types which are used in low level logic circuits, the 447A logic diode and the 449A level shifter diode.

The logic diode (447A) switches milliampere currents in much less than a millionth of a second to perform the required logic functions. The switching speed limitation for these diodes results from charge storage effects which delay the change from on to off by a few nanoseconds. However, this effect does not limit the speed of the low-level logic circuit which depends on other, slower operating, components.

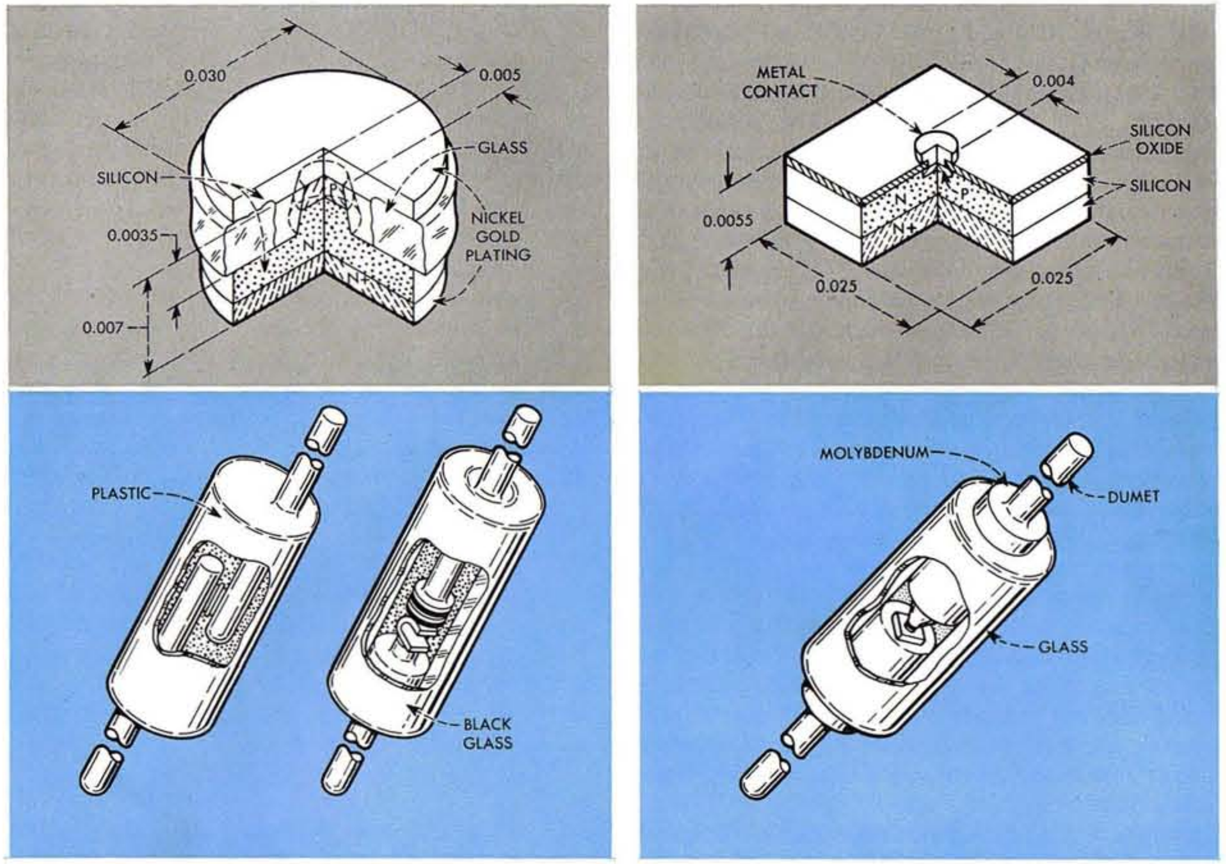
The evolution of the logic diode is similar to that of the logic transistor in that a mesa type is being replaced by a planar design. Both an early design and the present structure utilize a mesa type "pinhead" diode element (RECORD, *September 1963*). This diode element (see the drawing on page 266) is similar to a miniature pill box. It is composed entirely of silicon, glass and plated metal contacts and is particularly noted for being the first diode design to achieve a low failure rate at extremely high temperatures. The early design included soft soldered lead connections to the "pinhead" diode element with a plastic molding. This method of connecting leads to the "pinhead" was not completely reliable, and in some cases electrical contact was intermittent.

The present design, a "pinhead" encapsulated in a dark glass cylinder, alleviates the problem. The "pinhead" element is eutectically bonded to the end of a dumet (copper-clad nickel-iron alloy) lead having a pre-sealed glass bead; a U-shaped spring is welded to another dumet lead having a pre-sealed glass bead; and a dark glass cylinder is high temperature sealed to the beads and around the "pinhead" and U-spring assembly. During sealing, a gold-silicon bond is made between the U-spring and the "pinhead" to complete the electrical connections.

The future of the logic diode for No. 1 ESS seems to be the planar structure, the 458C. (See the drawing on page 266.) This recently developed model consists of a planar diode element which is bonded between two molybdenum cylinders during high temperature sealing within a glass cylinder. Dumet leads are welded to the outside ends of each molybdenum cylinder to complete the package. Because of the materials and processes used, this encapsulation is exceptionally well suited to modern reliability and quality control techniques which are carried out under conditions of high thermal and electrical stress. The 458C logic diode has electrical characteristics almost identical to those of the 447A and is easier to handle, harder to damage, and more reliable than any type which has been evaluated.

The level shifter diode (449A) is an essential component of the lowlevel logic circuit. It performs a battery-like function during transistor turn-off. Energy stored in it during forward conduction is used as a source of power to force the transistor to turn off in a fraction of the time it would take otherwise. After both transistor and diode have turned off, the circuit noise margin is greatly enhanced by the roughly two volts forward bias required to turn the diode on.

This diode (see the drawing on page 267) is composed of a stack of three silicon diode wafers simultaneously thermocompression bonded together to a gold plated kovar stud to which a gold plated nickel lead has been welded. The



Evolution of the logic diode from the mesa pinhead, left, the presently used design, to the planar structure, right, which was recently developed and is the future design for the No. 1 ESS logic diodes.

stud-wafer-lead assembly is welded to a kovar can which includes a high-temperature-glass sealed kovar tubulation. A cold weld pinch off of the tubulation includes the upper end of the gold wire, previously thermocompression bonded to the top of the diode element. This completes the internal electrical connections and makes the final vacuum-tight seal. A gold plated nickel lead with flattened and shaped end is welded to the end of the tubulation to complete the diode assembly. The use of these high melting point materials forms a mechanically rugged and highly reliable package which is used for a large family of diode types.

About two thirds of the remaining diodes in a No. 1 ESS office are the medium speed, medium current, switching type designated 446A. It is used in over 50 different circuit configurations where currents from tens to hundreds of milliamperes must be switched in tens of nanoseconds or longer. Its "on" resistance is less than an ohm and its "off" capacitance is less than 25 picofarads. The structure for the 446A diode is nearly identical to that of the 449A level shifter except that a single diode wafer is used instead of the three deck sandwich.

Voltage regulators, the second category of diodes in No. 1 ESS, are used in relatively small numbers as voltage limiters and voltage control devices. Based in principle on the solid-state avalanche and zener phenomena, they provide a relatively constant voltage over a fairly wide range of values of reverse currents. (Avalanche and zener are breakdown mechanisms that produce an extremely large increase in current from a slight increase in voltage.) There are three types of voltage regulators characterized by different breakdown voltages. The encapsulation for these diodes is the same as for the level shifter diode type 449A and the medium current switching type 446A. (See the drawing page 267.)

Greater current carrying or power handling ability than the 446A diode provides is necessary in some places in No. 1 ESS, such as the twistor memory access circuits. A high-current diode, the 426AC, can switch currents in the ampere range in less than 100 nanoseconds. The active element in this diode is much like the 446A except that the junction area is about five times larger. The package, like the others we have described, is fabricated of only high temperature materials in order to achieve an extremely high degree of reliability.

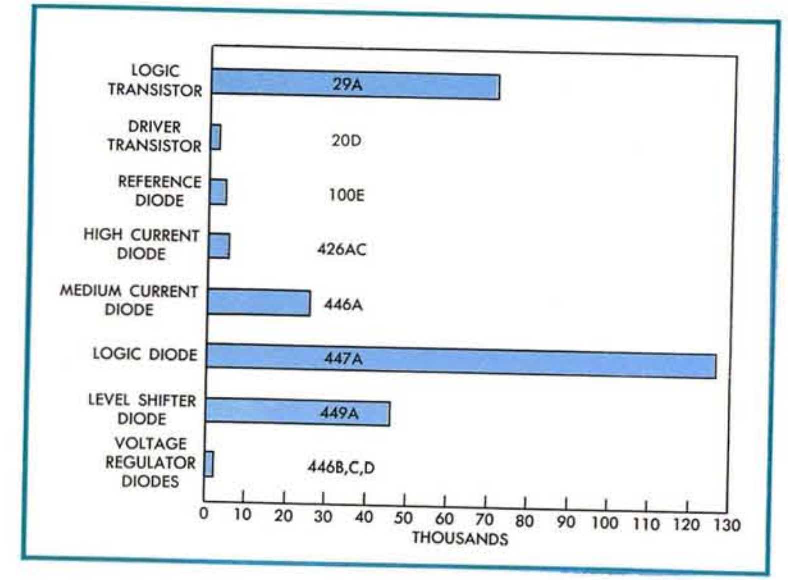
In a system as complex as No. 1 ESS, reliability, a key measure of performance in the telephone business, must be specially emphasized. Duplicate, parallel central control units are necessary to permit field modification without service interruption as well as to assure service in the event of equipment failure. Some duplication of peripheral system equipment is also used in No. 1 ESS. This increases the number of components in the office but it leads to an extremely high degree of telephone service reliability. However, even with duplicate critical units, the semiconductor devices must exhibit extremely high reliability.

The field trial of the prototype office at Morris, Illinois demonstrated about one transistor failure every three weeks. At first glance this is reasonable reliability; but for a commercial office it is quite inadequate. The Morris office served only 600 lines and contained about 12,000 germanium transistors, while a typical 10,000-line No. 1 ESS office contains more than 300,000 semiconductors. If No. 1 ESS transistors and diodes had the same failure rate as the Morris transistors they would fail at a rate of about one per day, thus creating a significant possibility that both of the parallel central controls might be unserviceable simultaneously.

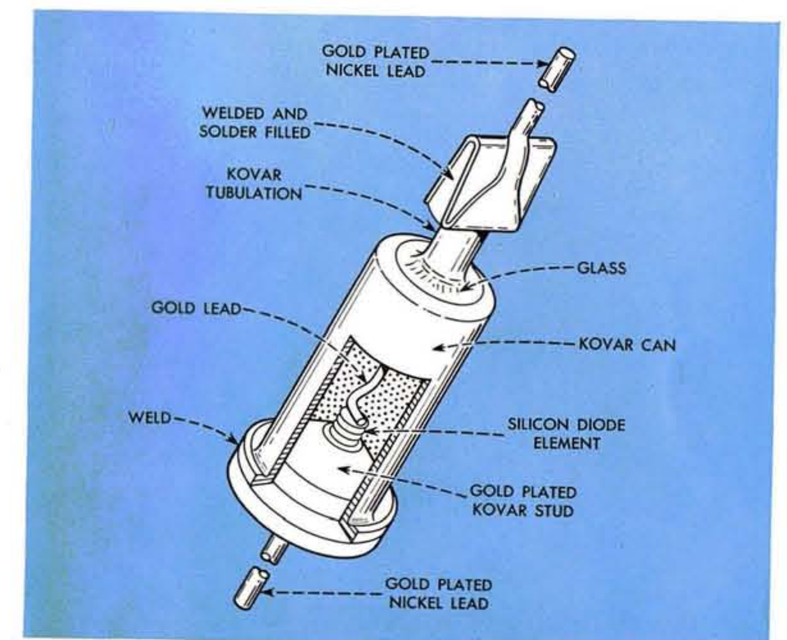
Great strides in semiconductor device reliability have been made since Morris. All of the transistors and diodes for No. 1 ESS are made by the newer diffusion technology and use materials which are compatible with high-temperature processing and modern reliability control techniques. Similar devices used in other major electronic systems have shown the reliability required for No. 1 ESS. It is clear that the No. 1 ESS device reliability objective will be met.

At both the Holmdel Laboratory experimental system, and during testing at the Succasunna office, the failure rate of semiconductors has been somewhat higher than the objective rate. However, this is largely the result of system testing and the rate of failures has decreased as the tests come closer to completion.

To sum up, the semiconductor devices of No. 1 ESS have been designed to achieve electrical characteristics suitable for broad uses—mechanical ruggedness to permit automatic circuit assembly; low cost to help achieve economical telephone service; and utmost reliability, reducing office maintenance and achieving the primary goal of accurate, reliable telephone service to Bell System customers.



Semiconductor devices in a typical 10,000 line office of No. 1 ESS.



Encapsulation design adopted for the level shifter diode, the medium-current switching diode and the voltage regulator diodes.

H. C. Przybysz, R. K. Voss, and T. E. Jackson (front to back) use the Central Control Manual Tester to test the No. 1 ESS installed for the C. & P. Telephone Co. at Chase, Maryland. The large book in the foreground contains program listings which are used to interpret the displays on the Tester lamp panels.

After all the circuits and devices have been fabricated and all the frames and bays have been assembled and wired, there remains a vital task—evaluation testing. At this point the hardware comes to life as a functioning system.

Testing the System

R. S. Cooper

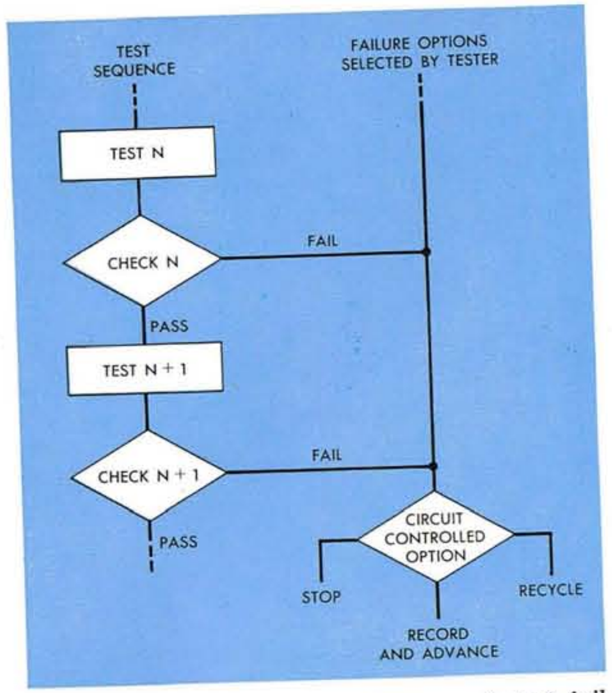
BEFORE No. 1 ESS can handle even the simplest telephone call, or execute the most routine maintenance procedure, it must be able to respond correctly to any logic problem presented to it. This ability must be tested and proved before the efficiency and accuracy of the program itself—which controls call processing—can be examined.

Any telephone system undergoes some testing at the factory and is run through a gamut of testing after it is installed in a central office building. This testing is performed even on the type of system that has been in production for many years. Its purpose is to ensure that each machine that comes off the assembly line will operate within the values set by the design specifications. A new system, however, may stand or fall on the first machine to be manufactured, because the effectiveness of the whole design is evaluated on the basis of that machine's performance.

Evaluation testing is a two-pronged attack. Its first point is straightforward. Every unit of hardware is tested both for its particular electrical or electronic functions—as a pulse inverter, or a delay network, etc.—and for its performance as part of an integrated system.

The second point of the attack is much more complex. An effective testing scheme must put a system through all its paces, so to speak. The range of tests must exercise the system in such a way that it demonstrates its response to all situations within the objectives of its design. A precise and meticulous testing scheme can do more than reveal shortcomings, conflicts, and errors in the design. It can suggest, by its results, changes in the design and sometimes in the design objectives.

In a program-controlled system, evaluation testing is equally concerned with hardware and the program. Although the call-processing programs of No. 1 ESS cannot be fully tested until all the system's circuits are operating, special test programs are a powerful tool. Hardware is the first concern and special "X-ray" programs were designed to examine all the hardware units of No. 1 ESS one at a time in sequence. These programs have a very high "resolving power;" that is, an ability to pinpoint the source of an indicated trouble.



The sequence of an X-ray program. A test failure causes a transfer to a common failure leg where one of three preselected options may take place. Stopping freezes the machine close to the failure point. "Record and advance" orders a print-out on the teletypewriter of data in the central control registers. "Recycle" continually repeats the test so that test personnel can stop and examine any part of a circuit with an oscilloscope.

Testing the Hardware

The system need be only partially installed to begin the sequence of X-ray programs. Only a program store and a central control that can communicate with each other are required. Before X-ray testing begins, however, the two units must have what is known as "basic sanity." That is, the program store must read out binary data without errors in its normal mode, and the central control must do two things. First, it must address the program store and add a binary 1 to a program address. This is a sign that it can execute successive program instructions. Second, it must transfer program control directly from one location to another in the program store, and it must perform a return-address option on a transfer. This is known as a "J" option, and it is the mechanism that shows a tester the point in the program at which a test fails.

Basic sanity is achieved through manual testing with a mobile, plug-in unit called the Central Control Manual Tester (CCMT). In essence, the CCMT simulates all the units of a working system by sending instructions to central control and governing their execution. Actually, the operator of the CCMT controls the clock circuits of central control and steps them along at manual speeds so that the instructions are carried out one at a time.

These tests look to a two-fold result which, incidentally, illuminates the psychological metaphor, "basic sanity." First, all the hardware necessary for communications between central control and the program store must be operating. The ability to communicate is a fundamental tenet of sanity. In addition to this, there must be no interference from hardware that is not required to operate. Noise, of course, can make chaos of an attempt to communicate.

Using the CCMT, the tester orders central control to send addresses to the program store and to receive words in return. Lamps on the test panel allow him to monitor the contents of a number of flip-flop registers of central control and the states of important circuit points. When the required minimum of basic sanity is achieved, the tester keys a direct transfer to the beginning of the X-ray program and the CCMT releases central control to proceed on its own. However, the CCMT remains attached to central control. During X-ray testing, it is called upon for three important functions.

First, the CCMT provides "flags" that signal central control to stop, or to transfer the program control to a fixed program address. The latter is called an "interrupt." The CCMT contains two program-address match circuits and each one continually compares the program address register with a pre-set number. When a match occurs, the circuits produce a flag. The flag can be used to stop central control in its tracks or to cause an immediate highest priority interrupt. Two memory-address match circuits in the CCMT perform the same operation on memory addresses read out as data.

Second, the CCMT is a data input to central control. Two 24-bit switch groups transmit starting addresses and other data. They also function as control switches to cut in special parts of the X-ray program or to bypass others.

Third, the CCMT continuously monitors central control and displays information on lamp banks. (The unit mounts about 450 lamps.) Lamp indications persist if central control is stopped, and the test operator can test them manually. One lamp bank displays the contents of any desired 24-bit word in the system memory.

The X-ray program consists of a series of

alternating checks and responses. An accurately performed exercise produces a specific result and the check affirms it. If a failure occurs, the machine executes a transfer with a J option and turns control over to a point in the program known as the common failure leg. (See the drawing on page 270.) A program address match circuit set in this leg stops central control. The tester, signaled by the J option lamps on the control console, then gives control of the program to the CCMT.

To clear up the trouble, the program is returned to the test on which the failure occurred. (A lamp group on the CCMT displays the address at which the J option was executed.) The operator now controls the clock circuits and guides central control step-by-step through a repeat of the test. He may use the interrupt to cause the system to cycle repeatedly through the program block in which the failure occurred while the suspected circuits are examined with an oscilloscope. A CCMT match circuit synchronizes the scope and the program.

After the X-ray program has exercised the program store and central control in all their possible circuit combinations, other system units are brought in. The first of these is the central pulse distributor. Again the X-ray program sends orders, and determines the internal condition of the unit from its response. This testing proceeds, in order, through the call stores, the network frames, and all other peripheral units in the system. A specific block in the X-ray program covers each unit.

All the major units of the system, are, of course, duplicated. But the testing to this point covers only one half of the system and takes no account of the other. In fact, the system is considered as two independent halves, and each is tested individually. When all the units have been tested singly, however, the duplicating scheme comes under scrutiny. Duplication schemes vary with different units. Some are simple—the unit may have access to either of two communication bus cables. Other are complex—for example, there are two complete central controls each with a full complement of hardware. In this case, both units are put through the same operation simultaneously and their outputs are matched to assure that they perform identically.

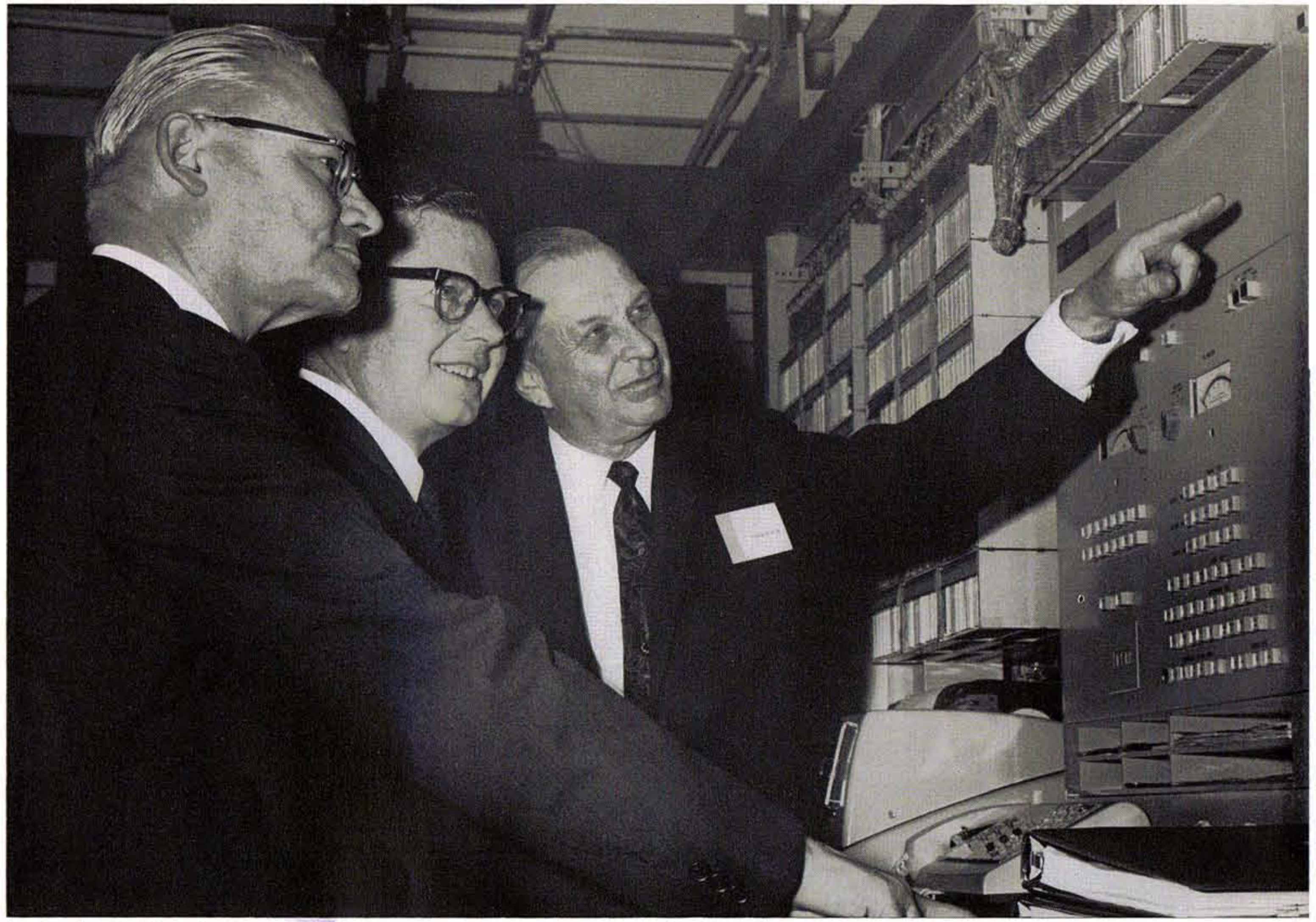
As X-ray testing progresses, a highly sophisticated system begins to emerge from the level of mere basic sanity. It can be called a bootstrap operation. The first tests in the program's repertory clear some units of hardware which can be used in subsequent tests. Early tests are quite simple, relying only on the hardware necessary to certify the basic sanity of the machine. Later tests are very sophisticated, because they may call on a growing amount of hardware and form complex circuit combinations.

If the motive behind this testing were merely to uncover faulty hardware, wiring errors, and similar faults, the X-ray program would be a needlessly complex procedure. But the power of the X-ray program lies in its critical perception, the ability to constantly compare an image of the system as it should work with the actual performance of the hardware. Common errors would be revealed by something as simple as continuity testing on circuits. But there may be a noise pickup or crosstalk between leads or groups of leads requiring that wiring be rerouted. A circuit may not handle its rated load under certain conditions, or a timing difficulty may lead to marginal operation in some circuits. All these possibilities are foreseen in the X-ray program. The scope of the tests and the range of operating conditions the X-ray program imposes on the system, should reveal the hardware's response to any event it may encounter in actual operating conditions.

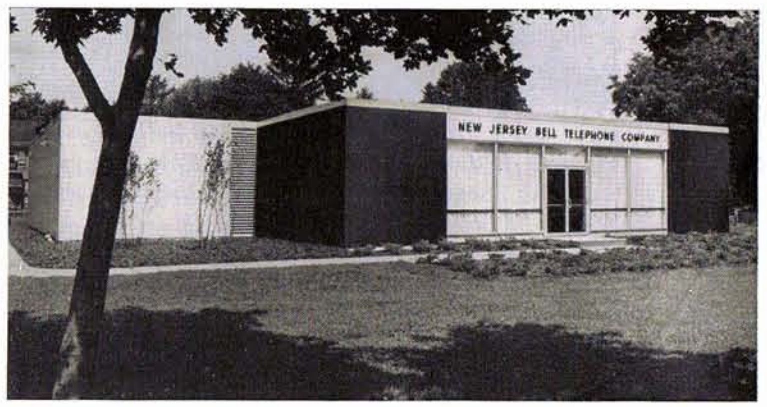
Testing the Program

Evaluation of the stored program itself, commonly called program debugging, follows X-ray testing. Its aim is to create complete harmony among the various sections of the program. An uncoordinated program disrupts the operation of No. 1 ESS, no matter how efficient its hardware. For instance, some program instructions depend on information gathered and stored by immediately preceding ones. However, testing may reveal timing difficulties; the first instruction may not be able to set up information in time for the second. Thus, the program may have to be rewritten so the two instructions do not follow in direct sequence. Other troubles yield only evanescent clues to their source and it may be difficult even to determine if they stem from the hardware or the program. Thus every step in program debugging demands close cooperation between a programmer and a system evaluation engineer who is thoroughly conversant with the hardware design.

Reduced to its simplest terms, program debugging is much like hardware testing—inputs are applied and outputs are checked. At the Succasunna office, input-output, control, and monitoring procedures are shared by the CCMT and the system's teletypewriter, and the control display and test panel of the master control center. At the Holmdel Laboratory, the system includes a pro-



Frederick R. Kappel, Chairman of the Board of A.T.&T., Richard Hughes, Governor of New Jersey, and E. Hornsby Wasson, President of the New Jersey Bell Telephone Co., (left to right) at the master control center of the No. 1 ESS central office at Succasunna.



The Bell System's first commercial electronic central office is housed in this building at Succasunna. It began serving 4300 New Jersey Bell Telephone Co. customers on Sunday, May 30, 1965.

United States Secretary of Commerce, John T. Connor at the Waldorf Towers, New York City receives an add-on conference call from Governor Hughes at Succasunna. Mayor Louis Nero of Roxbury Township was the third party in the call on No. 1 ESS.

Cut-Over At Succasunna

At 12:01 A.M. on Sunday, May 30, 1965 the Bell System's first commercial electronic central office, No. 1 ESS, began to serve 4300 customers in Succasunna, New Jersey.

The first official call through the system had been made two days before during the New Jersey Bell Telephone Company's dedication ceremonies. Governor Richard J. Hughes of New Jersey had initiated the system by adding-on John T. Connor, U.S. Secretary of Commerce to a conversation between him and Mayor Louis Nero of Roxbury Township, New Jersey. Mr. Connor was in New York City and the governor and mayor were at telephones in Succasunna.

Add-on is one of three system "memory services" now being tried by 200 customers served by the Succasunna office. Two more services will be added at a later stage of this trial. (*Features and Services* in this issue describes the five services.)

State, county, and local officials heard A.T.&T. Board Chairman Frederick R. Kappel describe the new installation as one of great significance in the history of communications. He said that No. 1 ESS will "open up an era of communications service that is more personalized, more human, than ever before by reason of its capacity to remember and do various special things that the individual customer wants it to do."

The electronic central office was developed, he said, to serve the future needs of the country for speedier and more abundant communications—in words, in data, in pictures, in symbols. This requires a more efficient and more versatile switching system than electromechanical devices permit.

"Not until the transistor was invented at Bell Telephone Laboratories in 1948 did electronic switching begin to emerge as a practical prospect," Mr. Kappel said. "Its inventors were investigating certain basic electronic characteristics of matter in the solid state. But whatever purpose beyond the search for knowledge they may have had in mind, there are today some 50,000 transistors in Succasunna's new central office—testimony, I think, to the value of so-called 'pure' research to growth and progress".

"Just as the Telstar satellite showed the way to new achievement in intercontinental services," Mr. Kappel said, "so this electronic central office is the forerunner of a new era of convenience for our neighborhoods and our nation. The strength of America's communications system lies in what we call the "switched network"—in the tremendous number of its inputs and outputs, its great speed and versatility, and its ability to connect any user anytime with any other. ESS is going to do this job for us better, faster and—in time—cheaper than ever before.

Succasunna is the first step in the nationwide conversion to electronic switching. Soon to follow are cutovers in Maryland, New York, and California. Mr. Kappel said that a dozen or more electronic offices are now in various stages of installation and that a new office will be installed every working day in the early 1970s. All switching in the Bell System, he said, will be done electronically by the year 2000.

THE AUTHORS

W. Keister

William Keister *(The Evolution of Telephone Switching)* is Director of the Electronic Switching Systems Engineering Center and is responsible for planning the engineering of electronic switching systems. Mr. Keister joined Bell Laboratories in 1930. His early work was on switching and signaling systems. He has organized and taught courses on switching circuit design to Laboratories personnel and is co-author of *The Design of Switching Circuits.* During World War II, Mr. Keister instructed Army and Navy personnel in operating and maintaining radar fire control equipment. He was appointed to his present position in 1958.

Mr. Keister received the BSEE degree from the Alabama Polytechnic Institute in 1930. He is a member of Eta Kappa Nu, Tau Beta Pi, Phi Kappa Phi, and the IEEE.

R. W. Ketchledge

Raymond W. Ketchledge *(From Morris to Succasunna)* is Director of the Electronic Switching Laboratory. He joined Bell Laboratories in 1942 and for four years was associated with military development of infrared detection and underwater sound systems. During the next six years he participated in the development of a submarine cable system and a broadband coaxial carrier system. In 1953, he was appointed Electron Tube Development Engineer and was responsible for the development of gas tubes and storage tubes. In 1954, he was appointed Switching System Development Engineer responsible for the development of electronic memories and switching networks for electronic switching systems. Mr. Ketchledge was made Assistant Director of Switching Systems Development in 1956 and was appointed to his present position in 1959.

Mr. Ketchledge received his BS and MS degrees from M.I.T. in 1942. He is a member of Sigma Xi and a Fellow of IEEE. He holds 51 patents with 6 pending.

John J. Yostpille *(Features and Services)* is Head of the Local Electronic Switching Planning Department. He is responsible for planning and setting engineering requirements for local central office applications of No. 1 ESS. He first joined Bell Laboratories in 1942 and in 1948 was in the first class of the Communications Development Training Program. He was first concerned with the design of toll switching equipment and after that with electronic switching. Before he was appointed to his present position he supervised a group engaged in systems planning.

Between 1942 and 1948 Mr. Yostpille was on leave of absence from the Laboratories during service in the Navy and studies at M.I.T.

Mr. Yostpille received the BS degree in Electrical Engineering from M.I.T. in 1948 and the

J. J. Yostpille

MSEE degree from the Polytechnic Institute of Brooklyn in 1955. He is a member of Sigma Xi and the IEEE.

Eugene H. Siegel, Jr. (Co-author *The Stored Program*) supervises a System Program Group concerned with the design of call processing programs for No. 1 ESS. Mr. Siegel joined Bell Laboratories in 1957 and for three years worked on the design of the barrier grid store circuits and system integration for the Morris trial ECO. Following that he was concerned with call store circuit design for No. 1 ESS and was appointed to his present position in 1963.

Mr. Siegel received the BS in EE degree in 1956 and the MS in EE degree in 1957 from Lehigh University where he held the Gotshall Scholarship in electrical engineering. He is a member of Tau Beta Pi and the IEEE.

E. H. Siegel, Jr.

S. Silber

A. H. Doblmaier

L. W. Stammerjohn

Sigmund Silber (Co-author *The Stored Program*) is a member of the Electronic Switching Programs Department, and has been engaged with the design of the executive control program for No. 1 ESS. Mr. Silber joined Bell Laboratories in 1961. While attending the Communications Development Training Program, he was engaged in various rotational assignments. Since then he has been concerned with the memory and program aspects of No. 1 ESS and certain data processing systems. He established program requirements for more than one data processor using the same memory. Most recently, he has been working with the system program test team for the Succasunna office of No. 1 ESS.

Mr. Silber received the B.A. degree in mathematics from Lehigh University in 1961. He is now studying toward the Ph. D. degree at New York University. Mr. Silber is a member of Phi Beta Kappa.

Anton H. Doblmaier *(The Control Unit)* is a member of the Electronic Switching System Design Department. For the last 10 years he has been concerned with switching development, particularly the logic design of control units for electronic switching.

Mr. Doblmaier joined Bell Laboratories in 1940. Until he transferred to his present assignment, he worked with an apparatus development group designing nonlinear networks involving copper oxide and thermistors. He holds one patent on a self-balancing thermistor.

Mr. Doblmaier was born in Munich, Germany. He entered this country in 1931 and received the B.A. degree from Columbia College in 1937 and the M.S. degree from the Columbia University School of Engineering in 1939 where he was a Pulitzer Scholar. He is a member of Phi Beta Kappa, Tau Beta Pi, and Sigma Xi.

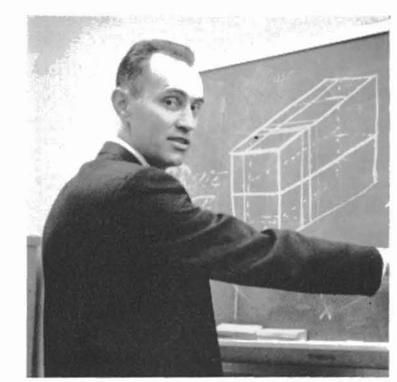
L. W. Stammerjohn (Co-author *Memory Devices)* is Head of the Magnetic Memory Department and is responsible for the development of magnetic memory and logic devices. He joined Bell Laboratories in 1940 and was first involved in the development of magnetic amplifiers, ferro-resonant devices, and transformers. Later he worked on the development of automatic tracking circuits for the Command Guidance System. He was appointed to his present position in 1958.

Between 1941 and 1946, Mr. Stammerjohn was on military leave of absence from Bell Laboratories serving on staff and command assignments in Iceland, England, and France. In particular, he served with the signal staff of the Ninth Air Force and was concerned with radar and communications for the control of fighter aircraft operations.

Mr. Stammerjohn received the BSEE degree in 1939 and the MSEE degree in 1940 from the University of Missouri. He is a member of Sigma Xi, Tau Beta Pi, Eta Kappa Nu, and a Senior Member of the IEEE.

R. H. Meinken (Co-author *Memory Devices)* is Head of the Magnetic Materials and Device Department at the Allentown branch of Bell Laboratories. He is responsible for the development of magnetic material and memory devices and other electronic materials.

Mr. Meinken joined Bell Laboratories in 1944 and for his first year was involved in the development of semiconductor devices. During the next four years, his major concern was the development of magnetic materials and



R. H. Meinken

memory devices and following that he spent two years on the development of solid state electro-optical devices.

Mr. Meinken received the B.Sc. degree in Ceramics from Rutgers University in 1949, the M.Sc. degree in 1951, and the Ph.D. in 1954. He is a member of the American Ceramic Society and Sigma Xi.

A. Feiner *(The Switching Network)* is Head of the Electronic Switching Networks Department and is responsible for the development of switching networks, trunks, and scanners, and for transmission aspects of No. 1 ESS. Since joining Bell Laboratories in

A. Feiner

1953, Mr. Feiner has been associated with various phases of electronic switching techniques.

Born in Vienna, Austria, Mr. Feiner did his undergraduate work at the Vienna Institute of Technology. He received the M.S. degree in Electrical Engineering from Columbia University in 1952. Mr. Feiner is a member of Sigma Xi.

D. H. Wetherell *(Mechanical Design)* Head of the Electronic Switching Equipment Department is responsible for the design and

D. H. Wetherell

development of equipment for No. 1 ESS. Mr. Wetherell joined the Western Electric Company in 1923 and Bell Telephone Laboratories in 1925. He worked on the development of equipment for all types of switching systems until World War II when he was appointed supervisor of a group designing airborne radar systems. After the war he supervised a group working on the development of equipment for toll telephone switching systems and later headed a group developing circuits and equipment for nation-wide dialing.

Mr. Wetherell received the B.S.E. degree from Lafayette College in 1923. He is a member of Tau Beta Pi.

J. W. Osmun (Co-author *Power Supply and Ringing and Tone Plants)* a member of the Power Systems Laboratory, specializes in electronic ringing and tone power plants. He joined Bell Laboratories in 1953 and graduated from the Communications Development Training Program in 1956. His early work at the Laboratories was in ringing power plants and transistorized dc-dc power converters.

J. W. Osmun

From 1943 to 1947 Mr. Osmun served as a parachutist with the U.S. Army, spending one year in the South Pacific theater of operations.

Mr. Osmun received the B.S.E.E. degree from the University of Nevada in 1953. He is a member of Phi Kappa Phi, Sigma Tau, and the IEEE.

J. R. Montana

J. R. Montana (Co-author *Power Supply and Ringing and Tone Plants)* a member of the Power Systems Laboratory, has been working on precise tone power supplies for No. 1 ESS, step-by-step, and No. 5 crossbar systems. Mr. Montana joined Bell Laboratories in 1944. He was first involved with the mechanical design and the preparation of manufacturing drawings of electromechanical equipment for various systems such as AMA. Later he was concerned with germanium and silicon purifying machines and then with rectifiers and inverters for development leading to the Morris trial. In 1961 he became a member of the Power Development Group and worked extensively on designing equipment for hardened sites and central offices.

Mr. Montana is a graduate of Brooklyn Technical High School and attended the Polytechnic Institute of Brooklyn.

R. L. Campbell (Co-author *A New Approach to System Maintenance)* is a member of the Electronic Switching System Center. He joined Bell Laboratories in 1960 and has worked since that time in the Electronic Switching Maintenance Planning Department at both the Whippany and Holmdel, New Jersey Laboratories. Since joining the Laboratories he has specialized in maintenance planning for No. 1 ESS. His work has involved planning automatic circuits and programs which allow the electronic system to find its own troubles.

R. L. Campbell

Mr. Campbell received the B.S. degree in electrical engineering from the University of Maine in 1960 and the M.E.E. from New York University in 1962. He is a member of Tau Beta Phi and Phi Kappa Phi.

Wendl Thomis (Co-author *A New Approach To System Maintenance)* is a member of the Electronic Switching Maintenance Planning Department. He joined Bell Laboratories in 1959 and was first involved with work on the maintenance dictionary for the Morris ECO trial office and with the Morris Switching Network Routine Tests. Since then he has been working on No. 1 ESS and has been responsible for the requirements and general design of the teletypewriter translations and the system maintenance dictionaries.

W. Thomis

Mr. Thomis received the B.S. degree in Mechanical Engineering from the Illinois Institute of Technology in 1956 and the M.S.M.E. degree from Purdue university in 1959. He completed the Communications Development Training Program in 1962.

Daniel H. Wenny, Jr. *(Some Magnetic Materials)* has been supervisor of the Metallurgical Development Group of the Metallurgical Research Laboratories for the last 20 years. In the last few years he has been responsible for work on various metal components for the twistor memory arrays and the ferreed crosspoints of No. 1 ESS. Mr. Wenny joined Bell Laboratories in 1930. His first assignment was studying methods of preparing permalloy dust for cores used in loading coils. In his present position he has worked on a wide variety of base and precious metal alloys for magnetic applications, contacts, springs, reed selectors, delay lines, and transmission lines.

D. H. Wenny, Jr.

Mr. Wenny received the degree of Metallurgical Engineer from Lehigh University in 1930.

M. L. Embree

M. L. Embree (Co-author *Semiconductor Devices*) supervises the Application Engineering and Reliability Group of the Semiconductor Device and Electron Tube Laboratory. He joined Bell Laboratories in 1951 and was first concerned with military systems development. Later, he was transferred to the Allentown Branch Laboratory and assigned to semiconductor device development. In 1955 he was appointed supervisor of a transistor development group working on point contact, alloy, and diffused transistors. He was appointed to his present position at the Laureldale Branch Laboratory in 1958.

Mr. Embree received the B.S. degree in electrical engineering from the University of Illinois in 1949 and the M.S. degree in 1950. He received an M.S. degree in Physics from Lehigh University in 1957.

J. Sevick (Co-author *Semiconductor Devices*) is supervisor of the Applications Engineering Group of the Semiconductor Device and Electron Tube Laboratory. He is concerned mainly with silicon transistors and integrated circuits. Mr. Sevick joined Bell Laboratories in 1956 and was first assigned to the development of high-frequency germanium and silicon transistors. Later he joined a systems group doing exploratory development work in high speed PCM. After that he was transferred to the Lauredale Branch Laboratory and supervised a group in applications engineering. He presently works at the Allentown Branch Laboratory.

During World War II, Mr. Sevick was a pilot and radar officer in the U.S. Air Force.

Mr. Sevick received the B.S. degree in Education from Wayne State University in 1940 and the Ph. D. degree in Physics from Harvard University in 1952. He is a member of a committee establishing an educational television station in the Lehigh Valley.

J. Sevick

R. S. Cooper *(Testing the System)* is a member of the Electronic Switching Evaluation Department. He has specialized in systems evaluation, working on the Holmdel experimental No. 1 ESS since 1960.

Mr. Cooper joined Bell Laboratories in 1954 and was enrolled in the Communications Development Training Program which he completed in 1957. During that time he worked on the design and development of military systems and PCM carrier systems. After these assignments, Mr. Cooper was concerned with the Morris trial ECO. He was involved in liaison with the Illinois Bell Telephone Company in preparation for the trial as well as with system evaluation.

Mr. Cooper received the A.B. degree in Physics from Williams College in 1952 and the MSEE degree from Dartmouth in 1954.

R. S. Cooper

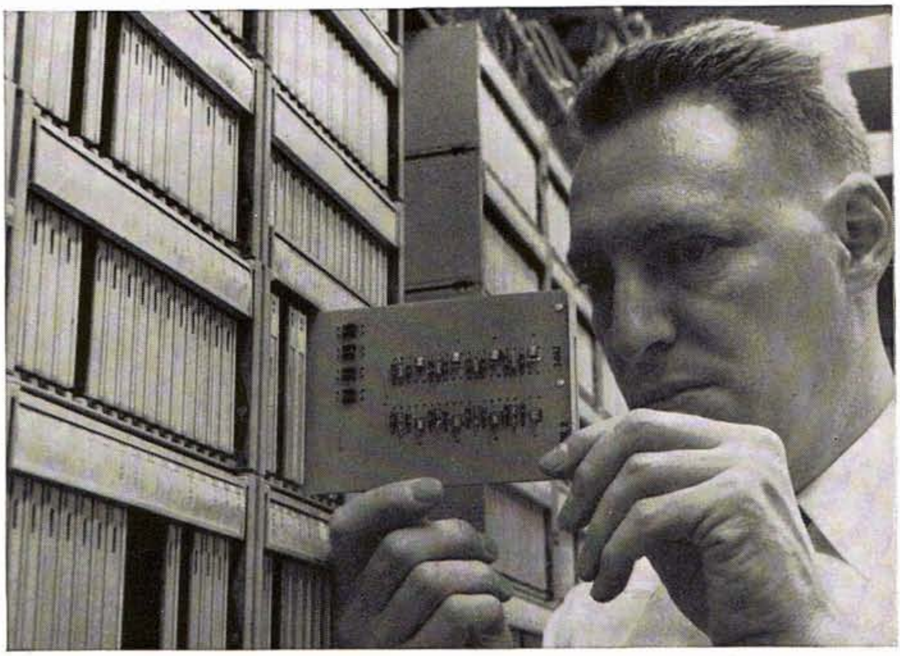
At the ceremony marking the cut-over of No. 1 ESS at Succasunna, New Jersey, A.T.&T. Board Chairman Frederick R. Kappel said:

"It would probably take a couple of hundred rooms of this size to accommodate all the people who in one way or another have contributed to this accomplishment — the scientists, and engineers, and craftsmen who developed, designed, and installed its hardware, the mathematicians and programmers who created its software."

The authors in this issue represent only a few of the groups at Bell Laboratories who contributed to the development of the new system. They should be considered only as spokesmen for the men and women, too numerous to name, whose active and enthusiastic cooperation made No. 1 ESS a success.

Report from

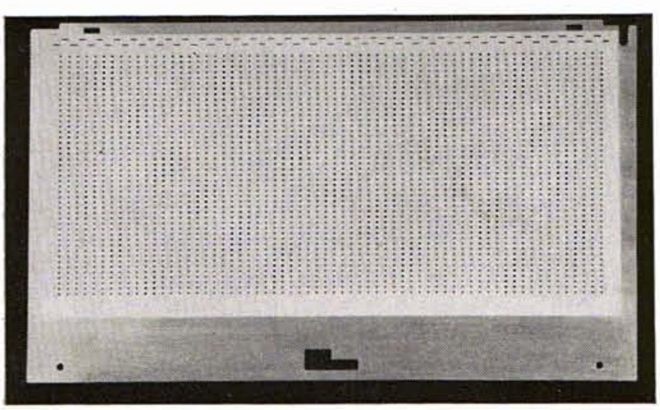
BELL LABORATORIES



B. G. Hemmendinger examines one of the digital circuit packages used in the central control unit of the new Electronic Switching System developed at Bell Laboratories. In these circuits, logic functions such as AND, OR, and AND-OR are built up with various combinations of a basic AND-NOT gate. About 27,000 transistors and 90,000 diodes are used in two duplicated central control units for one electronic central office.

Stored-program control—flexibility for telephone switching systems

Modern systems that switch your telephone calls use complex control equipment to operate the switches that make telephone connections. Such "common control" equipment is time-shared by many telephone lines. In electromechanical systems, common control apparatus consists of hardware—an array of hundreds of relays wired together to do the switching jobs of a particular telephone exchange.



Memory card, 6½ by 10½ inches, used for storing the ESS control program. Useful information (64 forty-four-bit words) is carried by the card in the form of magnetized spots ("zero") and unmagnetized spots ("one"). The random-access memory stores the control program and other data on 2048 such cards (131,072 words). The control instructions themselves require a minimum of 100,000 words.

By contrast, common control in the new Electronic Switching System (ESS) developed at Bell Laboratories is exercised by a multitude of general-purpose digital circuits whose actions are directed by "software"—programmed sequences of instructions stored in memory. The operation of ESS, including the specific telephone services provided, can thus be changed merely by changing the magnetization pattern of memory cards like that shown at left, with little or no hardware rearrangement or rewiring.

More specifically, ESS common control consists of an electronic data processor with a large memory. The memory contains instructions for processing all of the different kinds of calls handled by a central office. Guided by this stored program, the data processor receives and interprets dialed digits, sends signals to appropriate switches, and at the same time detects and diagnoses circuit malfunctions.

With this flexible common control, combining hardware and software, ESS can efficiently provide the various telephone services available today as well as any new services needed for the future.

Bell Telephone Laboratories

Research and Development Unit of the Bell System